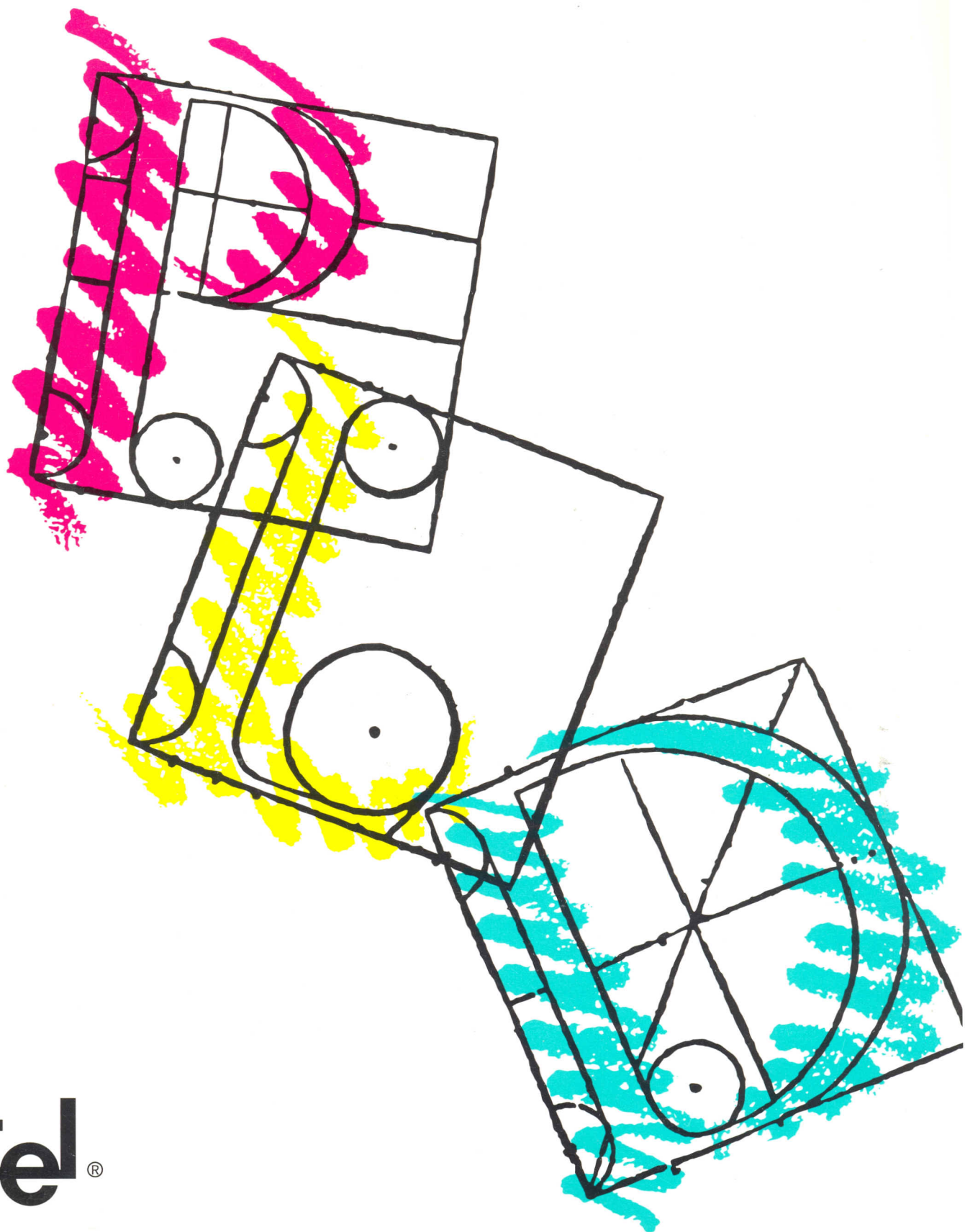


Intel Programmable Logic Devices
Family Product Brief/Q1 '94



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Intel Programmable Logic Devices Family Product Brief

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Intel Programmable Logic Devices Family Product Brief

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Product Highlights

- High Performance CMOS
- Predictability
- Low Power and Heat
- Reduced Ground Bounce
- Reduced Output Noise
- Excellent Metastability Characteristics
- High Quality and Reliability
- Development Tools Support

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- Predictability
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- Reduced Ground Bounce
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- High Quality and Reliability
- Development Tools Support



As you design higher-speed systems based on the Intel486™, Pentium™, and i960® microprocessors, you face an expanded set of design challenges. Intel CMOS PLDs and FPGAs are designed to help you master performance, predictability, heat dissipation, noise suppression, metastability, and quality and reliability.

In 1985, Intel began supplying Programmable Logic Devices with a series of 1.5 micron CMOS EPLDs. Four years later, Intel introduced the first members of its high-speed Programmable Logic Device (iPLD) family. With high speed, low power consumption, and a range of integration capabilities, these iPLDs are ideally suited for high-performance microcomputer system applications. Following growth and innovation on low density Programmable Logic Devices, Intel enhanced performance and predictability with the introduction of the FLEXlogic family of FPGA devices. As the Intel Programmable Logic and FLEXlogic families grow, they continue to present new opportunities for design innovation in high performance systems.

Performance

Highest performance CMOS PLD product line.

With computer systems becoming faster and smaller every day, the issues of integration, speed, and power consumption have an important impact on overall system performance. Intel's complete family of Programmable Logic Devices and Field Programmable Gate Arrays (FPGAs) meets the demand for small, fast, low-power systems. With system frequency support to 100MHz and logic propagation delays as low as 7.5 ns, Intel PLDs and FPGAs offer high performance at a full range of integration capabilities.

Fastest Performance in Programmable Electronics Performance Corporation (PREP) Tests

In recent PREP results, the first member of Intel's FLEXlogic family, the iFX780, was the strongest external performer of all devices compared in five of nine benchmark tests. The iFX780 also held top ranking in three more benchmarks.

External performance is clearly the most telling performance parameter. A device may operate fast internally, but in most real applications, the limiting performance is the system performance which is constrained by the speed at which signals can move on and off chip.



Operating at 80 MHz, Intel is the external performance leader in five PREP benchmark tests, including data path, small state machines, memory map, 16-bit counter, and 16-bit prescaled counter.

Proven Predictability

Intel is the only FPGA manufacturer whose internal and external performance is identical on every benchmark. This shows the consistency of high performance that the Intel FLEXlogic architecture was designed to deliver. With Intel's predictable performance you face little risk that your last minute FPGA design changes will cause major performance variants which delay you from the market.

The PREP results, highlighted here, demonstrate the predictability and ease of use of the FLEXlogic architecture given the repeatability of the numbers across all instances.

PREP Performance

Predictability

0 20 40 60 80 100

Intel iFX780-10

AMD MACH230-15

Altera EPM7128-1

QuickLogic QL12x16-2

Actel 1225-1

Xilinx x3190-3

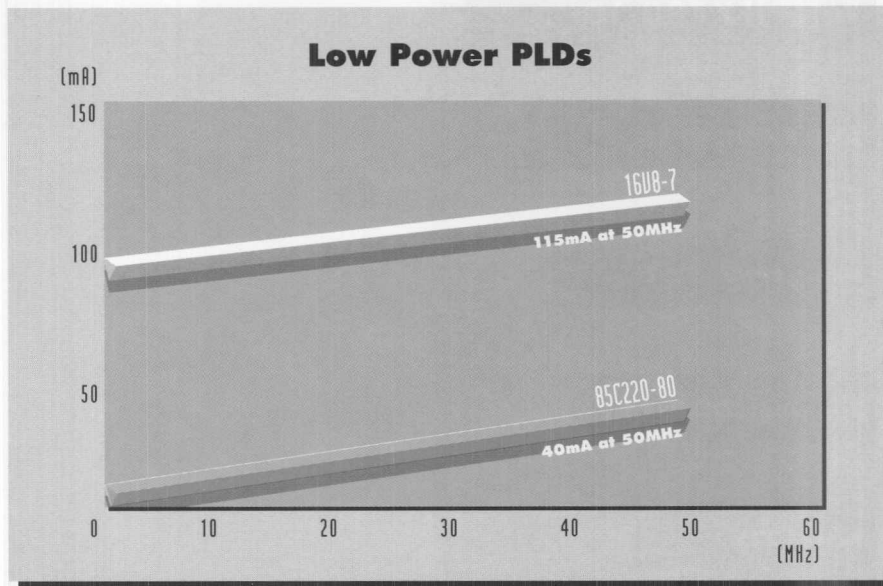
For a copy of the most recent PREP results, contact the PREP Administrator in California at (408) 356-2169.

Low Heat and Current Consumption

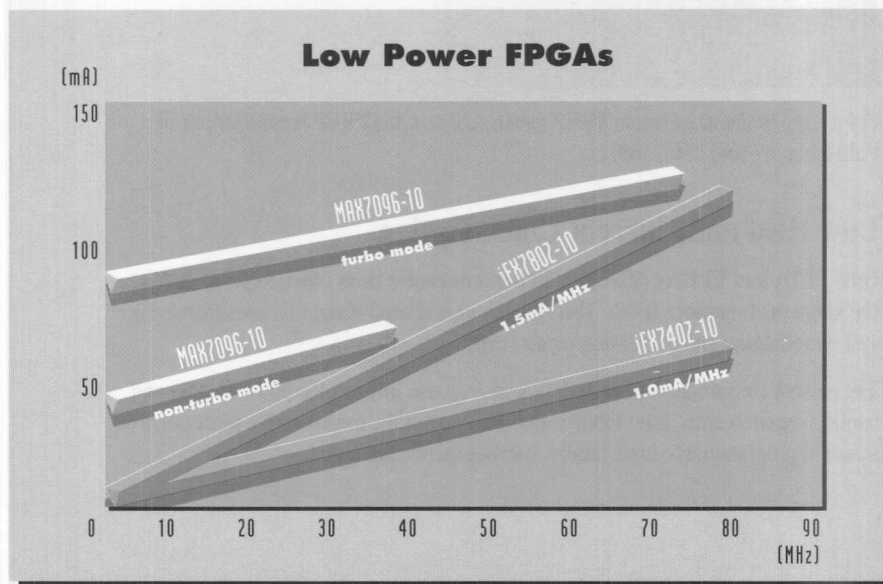
Intel PLDs and FPGAs run up to 50 percent cooler than other logic devices at the same performance level. This reduces heat-related system failures increasing system reliability and decreasing repair costs.

The current consumption of each device in a system impacts the power supply and cooling requirements. Intel FPGAs and iPLDs offer the lowest active power of any standard programmable logic family, without sacrificing speed.

It is well known that CMOS offers lower current consumption than standard bipolar PALs *, however it's also true that all CMOS is not created equal. Intel iPLDs operate at approximately half the power of GAL* devices. Also, most family members offer a programmable zero-power mode.



The Intel 85C220-80 provides lower power consumption than other devices which operate at the same speed.



FLEXlogic devices are lower power than competitive FPGAs over a large frequency range.

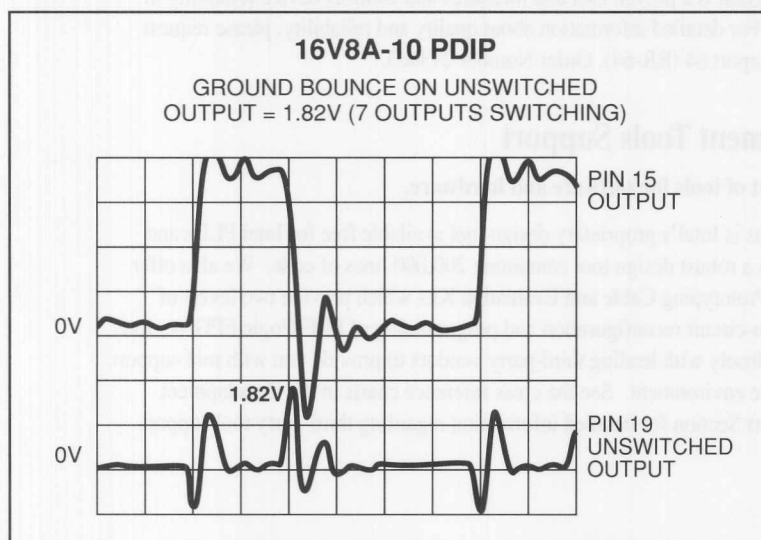
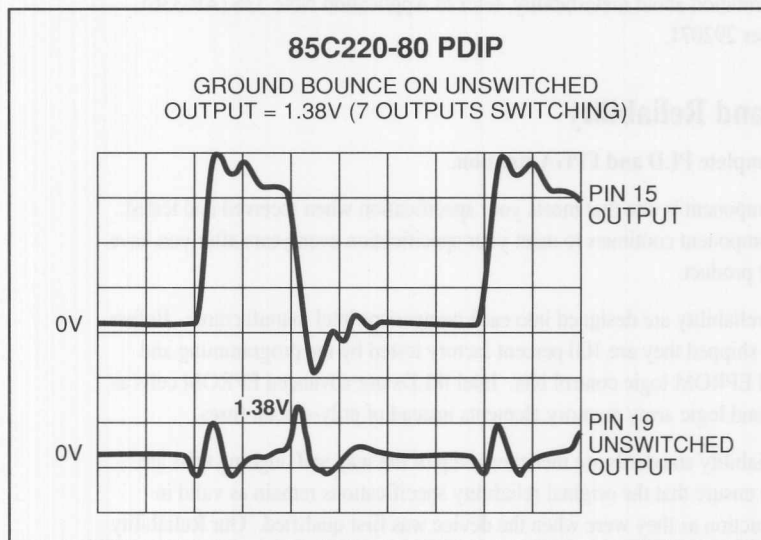
System Noise Reduction

Improve time-to-market by reducing debug time.

Noise control is an important consideration during system design since high-performance PLDs and FPGAs sometimes drive large loads at fast edge rates.

When designing with logic devices, supply line noise or ground bounce can affect the logical behavior of a circuit. Ground bounce is caused by switching loaded output pins very quickly. It intensifies as more outputs switch simultaneously.

To overcome this problem, the iPLD and FLEXlogic FPGA family of products are equipped with low noise output buffers that minimize transmission line effects and reduce ground bounce. For detailed technical information regarding ground bounce, refer to Intel Application Note 338 (AP-338), Order Number 292073.



Metastability

Superior metastability characteristics improve design reliability.

Metastability characteristics for programmable logic are determined largely by the semiconductor process used in manufacturing the device.

Edge-triggered registers inevitably enter a metastable state when driven by data asynchronous to the register clock. Using iPLDs with improved metastability characteristics increases system design reliability and decreases time to market.

Intel iPLDs and FPGAs are based on fast, CMOS EPROM process technologies which make them less likely to encounter metastable states than other devices. When metastability does occur, Intel PLDs and FPGAs recover quickly, keeping the output at a valid high or low (not oscillating) while recovery is occurring. For detailed information about metastability, refer to Application Note 336 (AP-336), Order Number 292071.

Quality and Reliability

Part of a complete PLD and FPGA solution.

A quality component is one that meets your specification when received and tested. A reliable component continues to meet your specification even years after you have shipped your product.

Quality and reliability are designed into each component Intel manufactures. Before our parts are shipped they are 100 percent factory tested by the programming and erasure of all EPROM logic control bits. Intel iPLDs use advanced EPROM cells as architecture and logic array memory elements instead of poly-silicon fuses.

Stringent reliability standards are met every step of the way and ongoing tests are conducted to ensure that the original reliability specifications remain as valid in volume production as they were when the device was first qualified. Our Reliability Monitor Program is a proven tool that measures and controls device reliability in production. For detailed information about quality and reliability, please request Reliability Report 64 (RR-64), Order Number 293003.

Development Tools Support

Complete set of tools for software and hardware.

PLDshell Plus is Intel's proprietary design tool available free for Intel PLDs and FPGAs. It is a robust design tool containing 200,000 lines of code. We also offer FLEXlogic Prototyping Cable and Evaluation Kits which provide two levels of support for in-circuit reconfiguration and programming of FLEXlogic FPGAs. Intel also works closely with leading third-party vendors to provide you with tool support in your native environment. See the cross reference charts in the Development Tools Support Section for detailed information regarding third-party tool support.

Customer Support

PLD Customer Support

Intel is committed to providing you with the support you need when you need it. With this goal in mind, we offer a variety of ways to access information, using mail, telephone, fax, modem, and PC.

Literature Support

For PLD literature, data sheets, or application notes, please call 1 (800) 548-4725 in the U.S. and Canada. To request information by mail, return the reply card located in this booklet.

FaxBACK System

Order documents by phone for prompt delivery to your fax machine. You can rely on FaxBACK 24-hours-a-day for the following information:

- Product literature
- Tools and technical support material
- Application articles
- New product announcements
- Design recommendations
- Stepping and errata notification

Just dial toll-free (800) 628-2283 or (916) 356-3105 and the user-friendly system will prompt you along. Have your fax number ready. In Europe, dial (44) 793 49 66 46.

Applications Support Hotline

The Technical Support Hotline is manned by applications personnel during normal business hours. You can leave a message during off-hours or when applications personnel are already handling calls. In the U.S. and Canada call (800) 628-8686. Assistance is also available through your local distributor or sales office.

Intel's Application Bulletin Board System

Key into our centralized Intel Applications Bulletin Board System (BBS) and pull up all the latest information on Intel's product line. The BBS can provide you with the following type of information:

- Software drivers
- Documentation
- New products
- Tools information
- Firmware upgrades
- Presentations
- Revised software

Intel's Application Bulletin Board System enables file retrieval and message/file exchange with our System Operator (Sysop) and File Operators (Fileops).

Just dial (916) 356-3600 on your modem, and the user-friendly system will prompt you along. In Europe, dial (44) 793 49 63 40.

For new users, the first log-in allows you to register with the system operator by entering your name and location. To access files on the BBS, log in again 24 hours later.

For immediate file access, call (800) 628-8686 or (916) 356-3104. For a listing of files available on the BBS, call FaxBACK at (800) 628-2283 or (916) 356-3105, order catalog #6. In Europe dial 44 (0) 793 496 340.

- Settings: 9600 baud, N, 8, 1
- Auto configuration supports 1200 through 9600 baud MODEMS.

CompuServe

Access to Intel technical support is available through the CompuServe PC-based information service. The Intel Access Forum on CompuServe includes a section titled Programmable Logic and FPGAs. It contains a data library of technical documents that can be downloaded to a PostScript printer, plus a messaging area for two-way communication between customers and Intel's technical support group. Even design files can be exchanged and reviewed. Intel checks the message area every business day and responds to each message within 24 hours of receipt.

If you are a CompuServe user, you may enter the Intel Access Forum by typing GO INTELACCESS.

High Performance FLEXlogic Devices

FPGA	Packages	Pins	Mcells (Regs)	I/O	t _{PD} (ns)	f _{CNT1} (MHz)	t _{SU} (ns)	t _{CO} (ns)	I _{OL} (mA)	I _{CC} (mA) @ Freq. (MHz)	Device Type/Application
FX780	N	84	80	60	10, 15	80	6.5	6.0	12	120 @ 80	Highest performance FPGA, SRAM option 3.3V support, JTAG interface. 5000 Gates
	KU	132	80	102	10, 15	80	6.5	6.0	12	120 @ 80	
FX740	N	44	40	30	10, 15	80	6.5	6.0	12	80 @ 80	Highest performance FPGA, SRAM option 3.3V support, JTAG interface. 2500 Gates
	N	68	40	50	10, 15	80	6.5	6.0	12	80 @ 80	

High Performance Industry Standard Devices

PLD	Packages	Pins	Mcells (Regs)	I/O	t _{PD} (ns)	f _{CNT1} (MHz)	t _{SU} (ns)	t _{CO} (ns)	I _{OL} (mA)	I _{CC} (mA) @ Freq. (MHz)	Device Type/Application
PLD22V10	P, N	24, 28	10	22	7.5, 10, 15	111	3	6	16	130 @ 15	High-speed, 22V10
PLDLV22V10	P, N	24, 28	10	22	15	50	10	10	16	35 @ 15	Low Voltage PLD — 3.3V Core Logic and I/O
PLD610	D, P, N	24, 28	16	20	10, 15, 25	74	7	6.5	12	105 @ 1	High-speed, general purpose; EP610/EP630 speed upgrade — Low Power Standby Mode
PLD910	D, P, N	40, 44	24	36	12, 15, 25	66.7	8	7	12	150 @ 1	High-speed, general purpose; EP910 speed upgrade — Low Power Standby Mode

Extended Feature Devices

PLD	Packages	Pins	Mcells (Regs)	I/O	t _{PD} (ns)	f _{CNT1} (MHz)	t _{SU} (ns)	t _{CO} (ns)	I _{OL} (mA)	I _{CC} (mA) @ Freq. (MHz)	Device Type/Application
85C220-80/66	D, P N	20 20	8	18	10, 12	80	7	5.5	12	60 @ 80	High-speed, 20-pin PAL/GAL superset (register optimized) — Low Power Standby Mode
85C220-100	N	20	8	18	7.5	100	4.5	5.5	24	115 @ 100	High-speed, 20-pin PAL/GAL superset (register optimized)
85C220-7/10	N	20	8	18	7.5, 10	74	7	6.5	24	105 @ 74	High-speed, 20-pin PAL/GAL superset (t _{PD} optimized)
85C224-80/66	D, P N	24 28	8	22	10, 12	80	7	5.5	12	60 @ 80	High-speed, 24-pin PAL/GAL superset (t _{PD} optimized)
85C224-100	N	28	8	22	7.5	100	4.5	5.5	24	115 @ 100	High-speed, 24-pin PAL/GAL superset (register optimized)
85C224-7/10	N	28	8	22	7.5, 10, 15, 25	74	7	6.5	24	105 @ 74	High-speed, 24-pin PAL/GAL superset (register optimized)
85C22V10	D, P N	24 28	10	22	10, 15	71.4	7	7	16	130 @ 15	High-speed, 22V10 superset; Invertible CLK, Expanded Feedback options

Packages: D = Ceramic Dual In-Line Package (Windowed for UV Erase)
N = Plastic J-lead Chip Carrier (One-Time Programmable)

P = Plastic Dual In-Line Package (One-Time Programmable)
KU = PQFP

*PAL is a registered trademark of Advanced Micro Devices, Inc.

*GAL is a registered trademark of Lattice Semiconductor, Corp.

Extended Feature Devices

PLD	Packages	Pins	Mcells (Regs)	I/O	t _{PD} (ns)	f _{CNT1} (MHz)	t _{SU} (ns)	t _{CO} (ns)	I _{OL} (mA)	I _{CC} (mA) @ Freq. (MHz)	Device Type/Application
5C031	D	20	8	18	40, 50	22	30	24	4	40 @ 10	General purpose PLDs; interface logic, state machine sequencers/controllers, Flexible I/O Architecture.
5C032	D, P	20	8	18	30, 35, 40	25	23	17	4	30 @ 25	General purpose PLDs; interface logic, state machine sequencers/controllers.
5C060	D, P N, M	24 28	16	20	45, 55	16.6	38	22	4	95 @ 96.6	General purpose PLDs; interface logic, state machine sequencers/controllers.
5C090	D, P N, M	40 44	24	36	50, 60	16.4	38	23	4	150 @ 16.4	General purpose PLDs; interface logic, state machine sequencers/controllers.
5C180	N, M	68	48	64	70, 75, 90	12.1	53	29	4	200 @ 12.2	General purpose PLDs; interface logic, state machine sequencers/controllers.

PLD	Packages	Pins	Mcells (Regs)	I/O	t _{PD} (ns)	f _{CNT1} (MHz)	t _{SU} (ns)	t _{CO} (ns)	I _{OL} (mA)	I _{CC} (mA) @ Freq. (MHz)	Device Type/Application
5AC312	D, P N	24, 28	12	22	25, 30	33.3	15	15	8	100 @ 33.3	Advanced architecture, general purpose: dual feedback, p-term allocation, 2 Set/Reset OE p-terms, synchronous/asynchronous clocks.
5AC324	D, P N	40, 44	24	36	25, 30	33	12.5	17.8	8	175 @ 33	Advanced architecture, general purpose: dual feedback, p-term allocation, 2 Set/Reset OE p-terms, synchronous/asynchronous clocks.

Packages: D = Ceramic Dual In-Line Package (Windowed for UV Erase)
N = Plastic J-Lead Chip Carrier (One-Time Programmable)

P = Plastic Dual In-Line Package (One-Time Programmable)
M = Military versions available

FLEXlogic Family Product Brief

Product Highlights

- Predictable 10ns pin-to-pin propagation delays
- 80 MHz system clock frequencies
- Flexible architecture:
 - 80 macrocells arranged in eight Configurable Function Blocks (iFX780)
 - 40 macrocells arranged in four Configurable Function Blocks (iFX740)
- Design flexibility
 - 5,000 equivalent logic gates or 10,240 bits of SRAM (iFX780)
 - 2,500 equivalent logic gates or 5,128 bits of SRAM (iFX740)
- Power management options minimize active power consumption:
 - 1.5 mA per MHz (iFX780)
 - 1.0 mA per MHz (iFX740)
- 100 percent connectable global routing matrix
- Fast 12-bit identity compare option
- In-system reconfigurable and programmable
- Selectable 3.3V or 5V I/Os
- 12 flexible clocking options
- 15ns SRAM
- Supports the JTAG 1149.1 boundary scan standard
- Supported by industry standard design and programming tools



Product Description

Designers have adopted Field Programmable Gate Arrays (FPGAs) to speed their products to market. Yet early FPGAs introduced new development problems, including complex new design tools, lengthy routing, uncertain timing and time-consuming device simulation. Intel's FLEXlogic family solves these problems.

Intel's iFX780 and iFX740 are the first two members of the Intel FLEXlogic family. Both combine the speed and ease-of-use of PLDs with the logic and density of FPGAs to give you the greatest design flexibility available.

The iFX780's flexible architecture contains 80 macrocells arranged in eight Configurable Function Blocks (CFBs). You can use each CFB as either a block of 10ns 24V10-like logic or as a block of 15ns 128 x 10 SRAM. The iFX740 contains 40 macrocells making it an ideal solution for designs that require all the benefits of the iFX780 but half the density.

To maximize fit and resource utilization, the FLEXlogic macrocells can allocate product terms without losing the donor macrocell as a resource or incurring additional delay. The devices also feature an on-chip 10ns 12-bit identity comparator for each CFB.

Both devices feature 12 clock options with a variety of set-up and clock-to-output timings that can be adjusted to meet your application needs. The FLEXlogic family delivers unmatched speed, with predictable 10ns pin-to-pin delays, even when implementing 16 product term equations. I/O pins can be configured as either 3.3V or 5V, allowing the device to serve as a bridge between subsystems of different voltages. With CFBs configurable as SRAM, you gain even more design flexibility. You don't have to include additional devices when you need memory.

Early FPGA products provided *either* in-system reconfiguration *or* on-chip non-volatile logic configuration storage. Intel FLEXlogic provides *both*. In-system reconfiguration offers design flexibility during prototyping, allowing you to test versions of your circuit design via its JTAG serial link as many times as necessary.

The iFX780 and iFX740 work with design tools you already use. Unlike other FPGAs which are limited to proprietary design tools, the FLEXlogic family is supported by leading third-party industry standard design entry/programming environments as well as Intel's PLDshell Plus development software. PLDshell Plus is available free of charge from Intel, Lit# 611942.

Features	Benefits
— 10ns at 80MHz system performance	— Predictable performance — Ease of design
— Flexible clocking options	— Ability to customize timing to your application
— Low power consumption	— Runs cool — Increases system reliability
— CFBs configurable as 15ns SRAM	— Increased design flexibility — Offers memory or logic in one device
— Reconfigurable	— Reusable during prototyping — Can modify in system
— Built-in CFB comparator	— Provides 12-bit identity comparisons with speed and efficiency

Package Options									
	Pins	Package	Macrocells	I/O	Inputs	Clocks	JTAG/VPP	VCC	GND
iFX740	44	PLCC	40	30	0	2	5	3	4
	68	PLCC	40	40	10	2	5	5	6
iFX780	84	PLCC	80	60	0	2	5	8	9
	132	PQFP	80	80	22	2	5	10	13

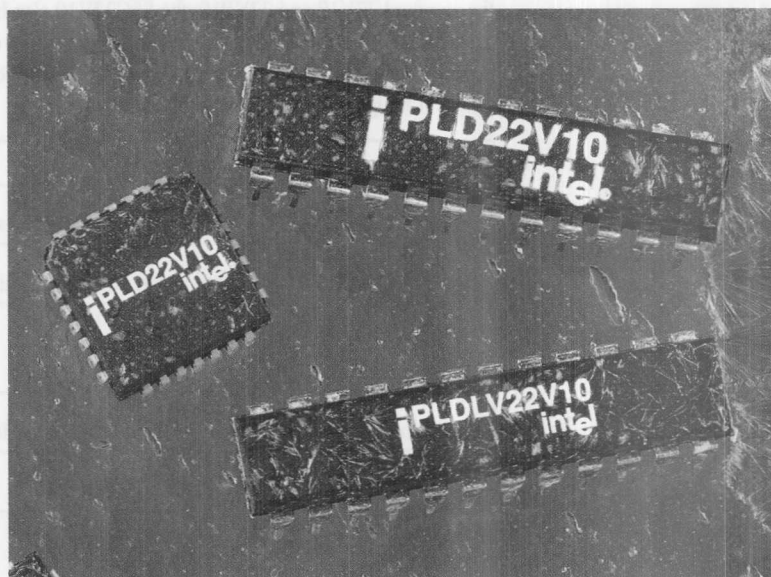
To request technical information, please return the reply card located within this booklet, or refer to the Information Resource card.

iPLD22V10 Programmable Logic Device

Product Brief

Product Highlights

- Pin-to-pin propagation delay of 7.5 ns
- Supports system clock frequencies of 111 MHz
- Fast set-up time (tsu) of 3 ns
- Enhanced integration capability incorporating 10 macrocells into a 24-lead device
- Consumes 40 percent less power than bipolar 22V10s
- Macrocell product-term allocation varies from 8 to 16
- Features 12 dedicated inputs and 10 I/O outputs
- Manufactured on Intel's 1-micron CMOS-IIIIE process
- Supports microprocessors running at 33 MHz or faster
- Available in a 24-lead PDIP package and a 28-lead PLCC package
- iPLDLV22V10 offers 3.3V core logic and I/O for low-power, low-voltage applications
Pin-to-pin propagation delays of 15ns, MAX Icc of 35 mA
- 85C22V10 offers added superset features including invertible clock and expanded macrocell feedback options. Both increase design flexibility.



Product Description

The iPLD22V10 is a high-performance CMOS PLD that is function-, lead-, and JEDEC file- compatible with industry-standard 22V10 devices. Existing 22V10 designs can be programmed into the iPLD22V10 using the same JEDEC file.

The iPLD22V10 accommodates logic functions with up to 22 inputs and 10 I/O macrocells. I/O macrocells feature 8 to 16 product terms for implementing logic and a separate p-term for output enable control. With a propagation delay (t_{PD}) of 7.5 ns the iPLD22V10 supports system clock speeds of over 111 MHz. This performance is achieved at a 40 percent power reduction compared to bipolar 22V10s and without the noise associated with CMOS GAL* devices. This allows the iPLD22V10 to implement embedded controllers, complex state machines and microprocessor-based system glue logic.

This device is manufactured on Intel's 1-micron CMOS IIIIE technology for low power consumption, making it easier to design for system power supply. As a low heat solution, it reduces temperature and eliminates fuse-related failures, improving board reliability and reducing replacement costs.

The iPLD22V10 supports any microprocessor running at 33 MHz or faster, including the Intel 386™, Intel486™, i960® CA/KX and i860™ microprocessors.

As a programmable device, the iPLD22V10 can help decrease your time to market. The same design tools used for the standard 22V10 can be used for designing with the iPLD22V10. Thorough design documentation and third-party programming support are also available.

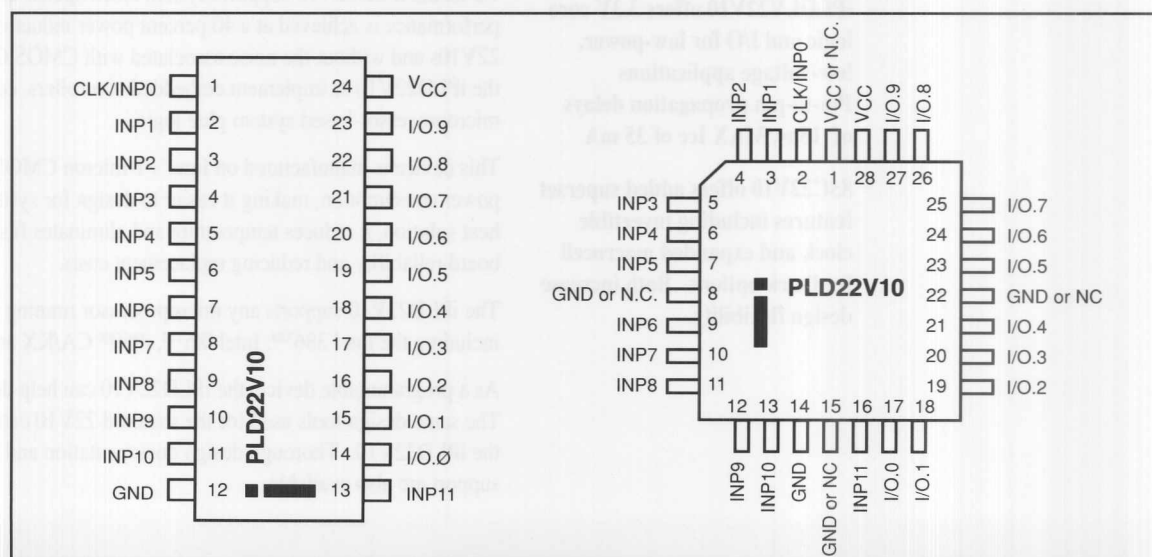
iPLDLV22V10 Low Voltage Programmable Logic Device: This device offers an industry-standard 22V10 architecture with 3.3V core logic and I/O's. Its fast propagation delay of 15ns with low maximum supply current of 35mA makes it ideal for battery operated and portable systems.

85C22V10 Programmable Logic Device: In addition to supporting the features of the standard 22V10 and 22VP10, the 85C22V10 also has the ability to invert the register clock on a macrocell by macrocell basis. The output feedback options have been expanded as well to support registered device outputs with pin feedbacks. This allows it to upgrade existing 22VP10 designs.

Features	Benefits
— 7.5ns t_{PD} , 3ns t_{su} , 111 MHz system clock speed support	— Compatible with high-speed system designs
— 10 macrocells, 12 dedicated inputs and 10 I/o leads	— High integration capability
— Socket and JEDEC compatible with industry standard 22V10 and 22VP10	— Can use same design tools
— Produced on Intel's 1-micron CMOS IIIIE technology	— 40 percent lower power than bipolar 22V10
— 3.3V core logic and I/O (iPLDLV22V10 only)	— Increases board flexibility
— 35mA max I_{cc} (iPLDLV22V10 only)	— Reduced heat dissipation, 1/4 power consumption of 5V counterparts
— Programmable inverted clock, configurable by macrocell (85C22V10 only)	— Greater design flexibility

Packaging

iPLD22V10	iPLDLV22V10	85C22V10
24-lead PDIP	24-lead PDIP	24-lead CerDIP
28-lead PLCC	28-lead PLCC	24-lead PDIP
		28-lead PLCC



Pinout Diagrams

To request technical information, please return the reply card located within this booklet, or refer to the Information Resource card.

iPLD610 Programmable Logic Device

Product Brief

Product Highlights

- Enhanced integration capability incorporating 16 macrocells onto a 24-lead device
- Fastest PLD of its integration capability — $t_{PD}=10$ ns, 100MHz registered performance
- Manufactured on Intel's 1-micron CMOS process
- Performance upgrade for the 5C060, EP600, EP610, EP610A, EP630, PALCE630, and multiple PAL-type/TTL logic devices
- Supports high performance microcomputer environments
- Features low power consumption requirements
- Available in a 24-lead PDIP package and a 28-lead PLCC package



Product Description

As the fastest CMOS Programmable Logic Device (PLD) of its integration capability, the iPLD610 is directly compatible with the Intel 85C060. The iPLD610 is a performance upgrade for slower devices based on the same architecture. It replaces the 5C060, EP600, EP610, EP610A, EP630, PALCE630, and multiple PAL-type/TTL logic devices.

The iPLD610 incorporates the industry-standard PLD architecture with the highest performance available. The device provides a t_{PD} of 10ns and supports registered designs at speeds of up to 100 MHz. Its high integration capability (16 macrocells) makes it an ideal replacement device for multiple PAL*-type/TTL logic devices. It helps reduce board space by integrating multiple PALs.

Manufactured on Intel's 1-micron CMOS process for low power consumption, the iPLD610 makes it easier to design system power supply. As a low heat solution, the iPLD610 reduces temperature and eliminates fuse related failures, improving board reliability and reducing replacement costs.

The iPLD610 supports any microprocessor running at 50 MHz or faster, including the Intel386™, Intel486™, i960® CA/KX and i860™ microprocessors. It is well-suited for embedded controllers, state machines, and general glue logic consolidation.

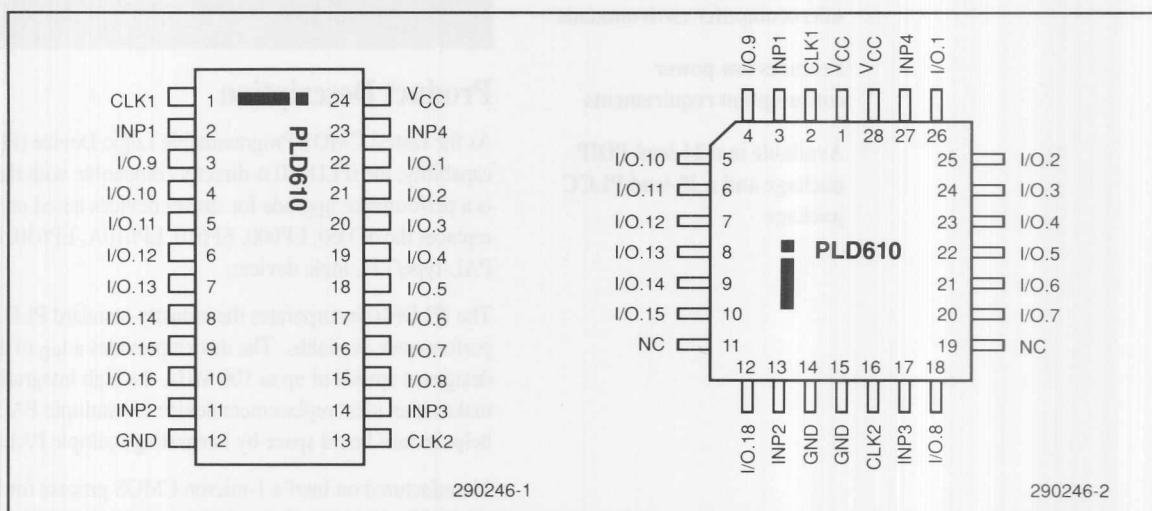
As a programmable device, the iPLD610 can help decrease your time to market. The same design tools used for the 85C060, the 5C060, the EP600 and the EP610, EP610A, and the EP630 can be used for the iPLD610. Thorough design documentation and third-party programming support are also available.

Features	Benefits
— Produced on Intel's CMOS technology	— High-speed performance, 10 ns t_{PD} , 100 MHz — Consumes less power and produces less heat than bipolar
— 16 macrocells, 16 I/O leads	— High integration capability, more outputs than the 22V10
— Registers configurable as D or T type	— Optimum flexibility for implementing complex state machines and counters
— Socket compatible with 85C060, 5C060, EP600, EP610, EP610A, EP630 and PALCE630	— Can use the same design tools — Industry-standard architecture
— Comprehensive design documentation and guidelines	— Ease of design — Faster time to market

Packaging

24-lead PDIP

28-lead PLCC



Pinout Diagrams

To request technical information, please return the reply card located within this booklet, or refer to the Information Resource card.

iPLD910 Programmable Logic Device

Product Brief

Product Highlights

- Enhanced integration capability (24 macrocells)
- Fastest PLD of its integration capability — $T_{pd} = 12$ ns, 62.5 MHz registered performance
- Manufactured on Intel's 1-micron CMOS process
- Performance upgrade for the 5C090, EP900, EP910, and EP910A
- Supports microprocessors running at 33MHz and faster
- Features low power consumption requirements
- Available in a 40-lead PDIP package, and a 44-lead PLCC package



Product Description

The iPLD910 is the fastest 40-lead CMOS PLD available. It is directly compatible with the Intel 85C090 and is a direct socket upgrade for slower devices based on the same architecture. It replaces the Intel 5C090, and the Altera EP900, EP910, and EP910A.

The iPLD910 Programmable Logic Device incorporates the industry standard PLD architecture with the highest performance available.

Manufactured on Intel's 1-micron CMOS process, the iPLD910 has a t_{PD} of 12ns and supports registered designs at speeds of up to 62.5 MHz. Its high integration characteristics (24 macrocells) allow designers to reduce board space by integrating multiple PALs* and complex PLDs.

The flexible architecture and high performance of the iPLD910 allow it to implement many designs targeted for the AMD MACH*110 device. It is well-suited for embedded controllers, state machines, and general glue logic consolidation. The iPLD910 supports any microprocessor running at 33MHz or faster, including the Intel386™, Intel486™, i960® CA/KX and i860™ microprocessors.

This device is manufactured on Intel's CMOS technology for low power consumption, making it easier to design system power supply. As a low heat solution, it reduces temperature and eliminates fuse related failures therefore improving board reliability and reducing replacement costs.

The iPLD910's reprogrammability can help decrease your time to market. The same design tools used for the 85C090, the 5C090, and the Altera EP900, EP910,

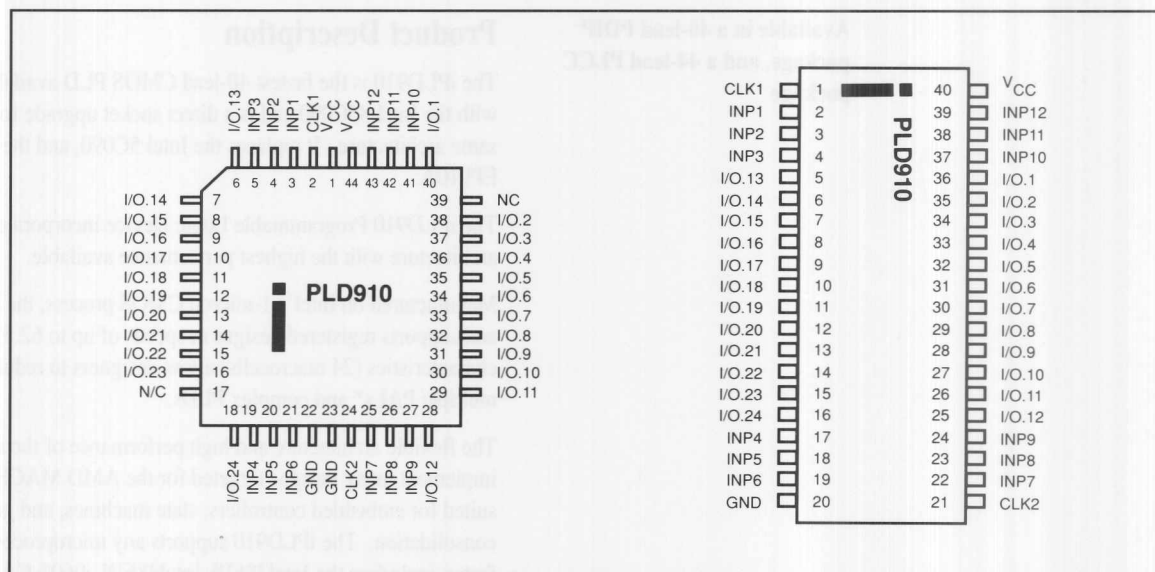
and EP910A can be used for the iPLD910. Comprehensive design documentation and third party programming support are also available.

Features	Benefits
— Produced on Intel's CMOS technology	— High-speed performance, $t_{PD} = 12$ ns 62.5 MHz registered performance
— 24 macrocells, 24 I/O leads	— High integration capability
— Socket compatible with 85C090, 5C090, EP900, EP910, and EP910A	— Can use the same design tools — Industry-standard architecture
— Registers configurable as D or T type	— Optimum flexibility for implementing complex state machines or counters
— Comprehensive design documentation and guidelines	— Ease of design — Faster time to market

Packaging

40-lead PDIP

44-lead PLCC



Pinout Diagrams

To request technical information, please return the reply card located within this booklet, or refer to the Information Resource card.

85C220/85C224 Programmable Logic Device

Product Brief

Product Highlights

- Superset of common 20/24-lead PALs/GALs
- Register-optimized 100, 80 and 66MHz devices for high-frequency programmable logic applications
- t_{PD} optimized 7.5ns and 10ns devices upgrade PALs/GALs with lower power consumption
- Extremely low output skew clock driver
- Minimizes transmission line effects through low noise output buffer design
- Reduces temperature thereby increasing reliability and reducing replacement costs
- Offers excellent metastability characteristics
- Eight macrocells with 8 p-terms each, selectable SOP invert and individual OE p-term per macrocell
- 85C220 has up to 18 inputs (10 dedicated and 8 I/O) and 8 outputs, 85C224 has up to 22 inputs (14 dedicated and 8 I/O) and 8 outputs
- Available in a 20-lead 300-mil DIP package and a 20-lead PLCC package



Product Description

The 85C220/224 uses advanced EPROM cells as architecture and logic control memory elements. Coupled with Intel's superior CMOS technology, the result is a device offers a fast t_{PD} with power consumption much lower than bipolar and CMOS devices of equivalent speeds. EPROM technology allows these devices to be 100-percent factory tested by programming and erasing all of the EPROM logic control elements.

The 85C220/224 is a logical superset of most high-speed 20- and 24-lead PAL*/GAL* devices. The I/O and logic sections of the device can be configured to replace or upgrade PAL/GAL 16V8 and 20V8 devices.

The 85C220/224 satisfies a wide range of programmable logic applications. This simple PLD is a high quality and low-cost alternative to PAL/GAL GAL 16V8 and 20V8 devices.

Its extensive list of features include high performance ($t_{PD} = 7.5\text{ns}$, $T_{su} = 4.5\text{ns}$, $T_{co} = 5.5\text{ns}$) and low power consumption (typical $I_{cc} = 40\text{mA}$).

Procurement: Highly cost effective. Enables wide-scale inventory reduction as a replacement for a long list of 20- and 24-lead PAL and GAL devices.

Design Engineering: Enhanced 8 macrocell architecture combines performance with design flexibility to help meet the most critical design specifications. In addition, low noise output buffers eliminate many spurious system noise problems that appear during debug and testing.

Quality and Reliability: Low power CMOS technology operates at cooler temperatures improving overall power consumption and reliability.

Manufacturing: Multiple package offerings add flexibility to high-volume manufacturing lines. Improved system quality reduces end-product test failure and rework.

Applications: The fast t_{PD} of 7.5ns, and the high F_{max} of 100 Mhz make the 85C220/224 ideal for designs that demand high speed, low power and low noise. Frequent applications include advanced microprocessor systems, PC expansion cards and peripheral products, mobile systems, communications, and general purpose digital design applications.

High Frequency/Low Output Skew Clock Driver

Compared to industry clock drivers, the 85C220/224 (-100 and -10) displays dramatically reduces output pin skew. With high performance systems relying on increasingly faster clocking frequencies, managing the timing of high frequency system clocks is now more important than ever. Whether the configuration is combinatorial (as with a clock driver) the output skew (T_{OS}) is typically less than 250 pico seconds! The extremely low output skew of the 85C220/224 makes the device ideal for a variety of high frequency system clock related applications including Pentium™ microprocessor, Intel486™ and PCI Bus designs. The 85C220/224 delivers the flexibility of programmable logic and the industry's lowest output skew — at a very attractive price.

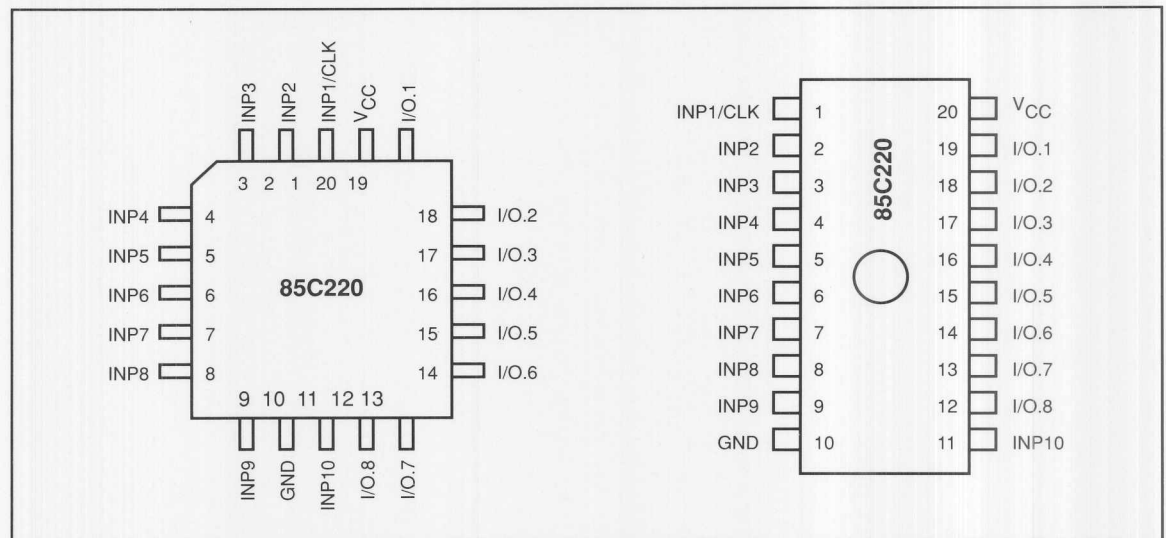
Features	Benefits
— 20- and 24-lead PAL/GAL superset	— Provides a one-part-fits-all solution that reduces inventory and paperwork
— High performance based on Intel's CMOS EPROM technology	<ul style="list-style-type: none"> — Operates at up to 100 MHz max frequency with external feedback, and 115 MHz with internal feedback for high performance registered applications — Fast t_{PD} of 7.5ns for high performance combinatorial applications — Low programming fallout, high reliability — All packages are 100 percent testable. The CerDIP package is reprogrammable — Provides excellent metastability characteristics — Eliminates fuse-related failures
— Lower power consumption	<ul style="list-style-type: none"> — Runs cooler and increases overall design reliability — Standby Mode for power critical applications (80 and 66 MHz)
— Low noise output buffer	<ul style="list-style-type: none"> — Minimize transmission line effects — Reduces ground bounce

Packaging

20-lead 300-mil CerDIP 85C220

20-lead 300-mil PDIP 85C220

20-lead PLCC 85C220



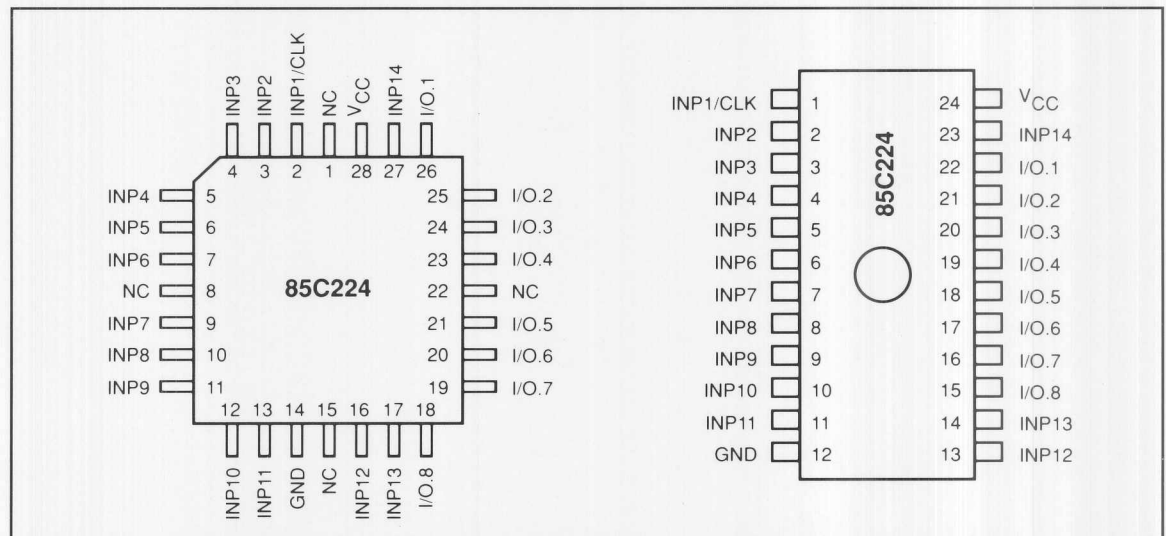
85C220 Pinout Diagrams

Packaging

24-lead 300-mil CerDIP 85C224

24-lead 300-mil PDIP 85C224

24-lead PLCC 85C224



85C224 Pinout Diagrams

To request technical information, please return the reply card located within this booklet, or refer to the Information Resource card.

Pinout

34-Pin DIP (P/N: 88C120)
34-Pin PLCC (P/N: 88C120)



88C120 Pinout Diagram

Pinout

34-Pin DIP (P/N: 88C121)
34-Pin PLCC (P/N: 88C121)



88C121 Pinout Diagram

Advanced Architecture PLD Family (5AC312/5AC324) Product Brief

Product Highlights

- Programmable low-power option for "stand-by" operation
- High-performance LSI semi-custom logic alternative for low-end gate arrays, TTL, and 74 HC- or 74HCT SSI and MSI Logic, and PLDs
- High speed t_{PD} 25 ns, 66MHz performance pipelined, 33.3 MHz with feedback
- Flow-through input or global CLK pin; 1 flow-through input or global ILE/ICLK pin
- Programmable AND, allocatable OR design allows up to 16 product terms per macrocell
- Software-supported product term allocation between adjacent macrocells
- Programmable output registers configurable as D, T, JK, or SR types
- Dual feedback on all macrocells for implementing buried registers with bidirectional I/O
- 2 product terms on all macrocell control signals
- UV erasable (CerDIP) EPROM technology or OTP
- 100 percent generically tested EPROM logic control array



Product Description

Intel's advanced architecture, general purpose CMOS PLD (Programmable Logic Device) Family represents an innovative approach to overcoming the primary limitations of standard PLDs.

Due to proprietary I/O architecture and macrocell structure, these PLDs are capable of implementing high performance logic functions more effectively than previously possible. They feature dual feedback, p-term allocation, set/reset/OE p-terms, programmable inputs, and synchronous/asynchronous clocks.

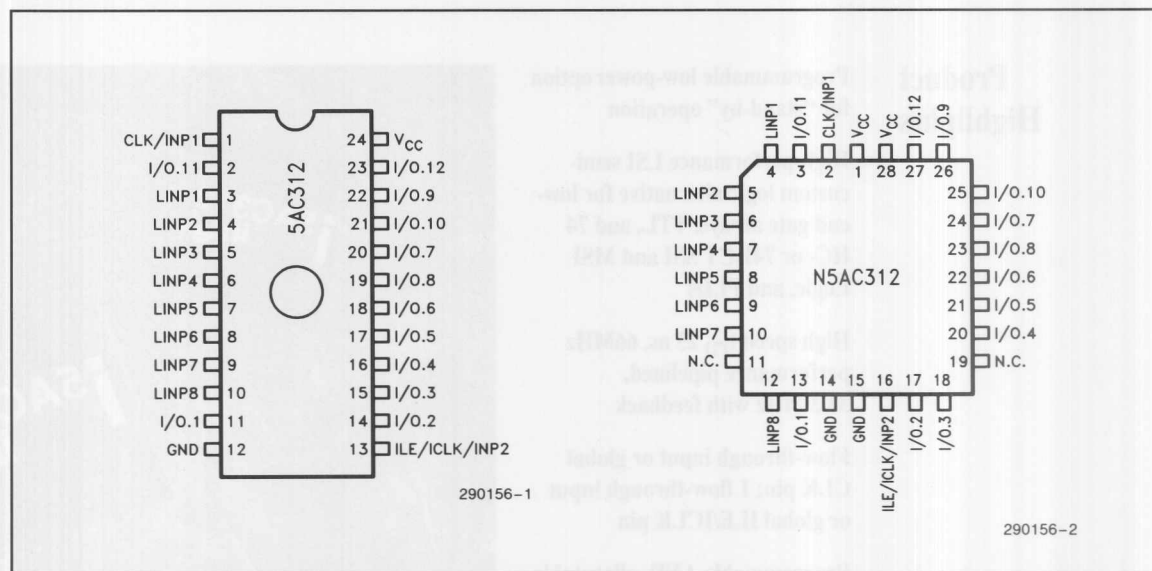
They can be used as an alternative to low-end gate arrays, multiple programmable logic devices or LS-, HC- or HCT SSI and MSI logic devices. Input and macrocell features for the 5AC312 and 5AC324 are a superset of features offered by other PLD-type products.

These devices use advanced CMOS EPROM cells as logic control elements instead of poly-silicon fuses. This technology allows these PLDs to operate at levels necessary in high performance systems while significantly reducing the power consumption. Their programmable standby function reduces power consumption to almost "zero" in applications where a slight speed loss is traded for power savings.

Packaging

24-lead PDIP/CerDIP

28-lead PLCC

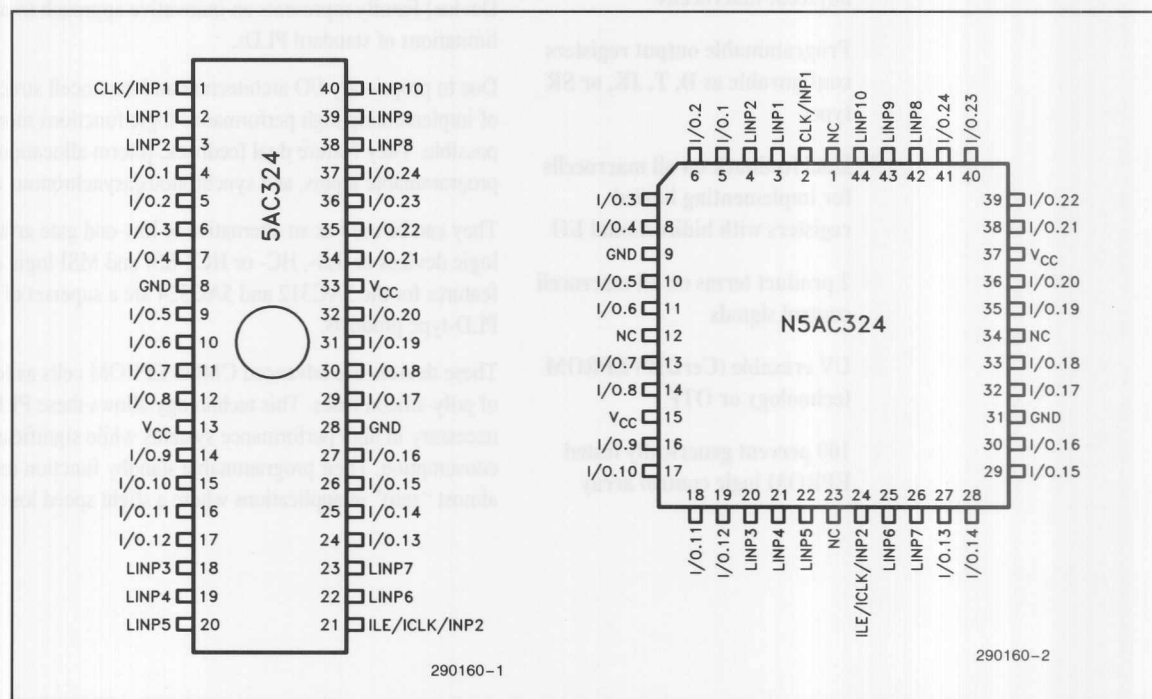


Pinout Diagrams

Packaging

40-lead PDIP/CerDIP

44-lead PLCC



Pinout Diagrams

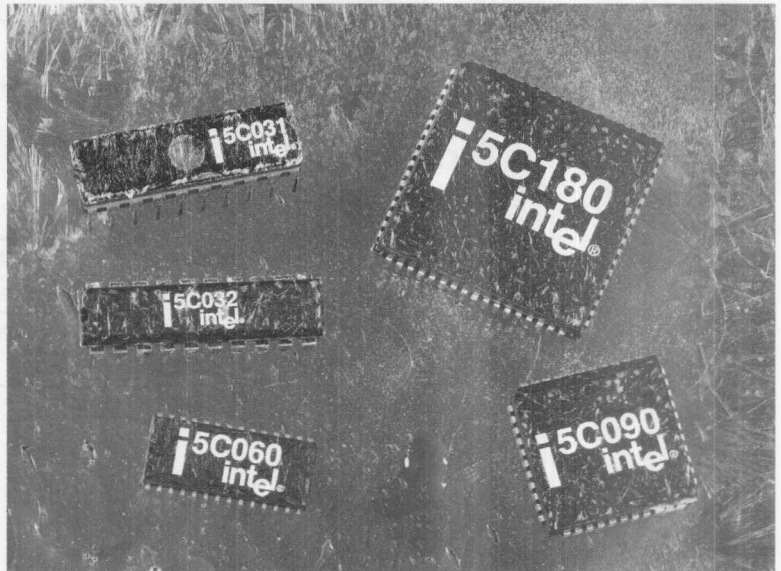
To request technical information, please return the reply card located within this booklet, or refer to the Information Resource card.

5CXXX Standard Architecture PLDs

Product Brief

Product Highlights

- 100 percent compatible with EP310, EP320, EP600, EP900, EP1800
- High performance LSI semi-custom logic alternative to low-end gate arrays, TTL and 74HC SSI and MSI logic
- 8 to 48 macrocells
- Low power standby current
- CMOS EPROM-based
- Programmable clock system



Product Description

Intel's family of standard architecture PLDs is 100 percent compatible with the EP310, EP320, EP600, EP900, and EP1800. The Intel 5CXXX family uses CMOS EPROM cells as logic control elements instead of fuses. This reduces the power consumption of PLDs to less than 20 percent of a comparable bipolar device without sacrificing performance. In addition, the use of Intel's advanced 1-micron CMOS EPROM process technology enables greater logic densities to be achieved with superior speed and low-power performance over other comparable devices. EPROM technology allows these devices to be 100 percent factory tested by programming and erasing all the EPROM logic control elements.

For ease of design and fast time to market, Intel provides a full library of design entry, simulation, compilation and programming tools for the PLD family of products. An aggressive program of third-party design support is also in place with vendors like DATA I/O, Logical Devices, Viewlogic, STAG, OrCad, and Omaton.

Features	Benefits
— Industry-standard architecture	— 100% socket compatible with EP310, EP320, EP600, EP900, EP1800
— Programmable low power option	— Runs cool, thereby increasing system reliability
— Dedicated fabrication resource	— Assurance of long-term product availability

Packaging

Package Options

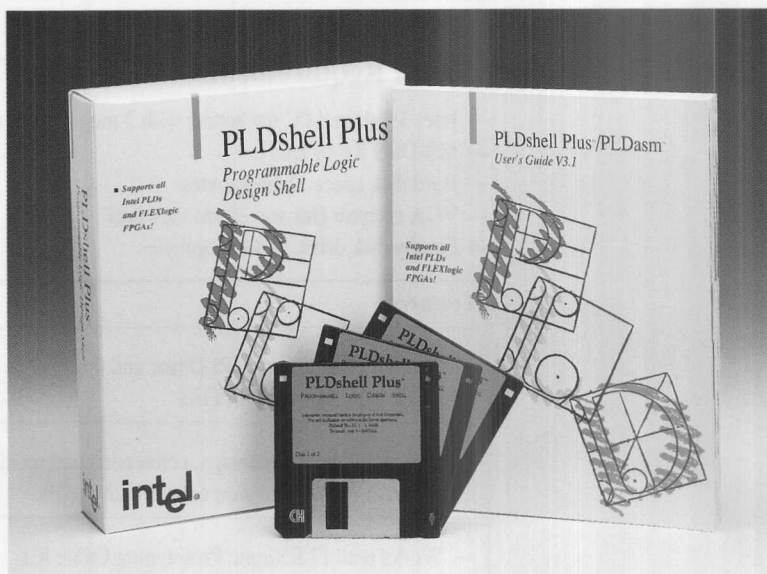
Package	5C031	5C032	5C060	5C090	5C180
CERDIP	20-PIN	20-PIN	24-PIN	40-PIN	
PDIP		20-PIN	24-PIN	40-PIN	
PLCC			28-PIN	44-PIN	68-PIN

To request technical information, please return the reply card located within this booklet, or refer to the Information Resource card.

PLDshell Plus Product Brief

Product Highlights

- Supports fitting to the iPLD line and the FLEXlogic family of FPGAs
- Easy-to-use menu interface with extensive help and on-line technical support information.
- Hierarchical design entry allows better management of large designs
- Extensive library of tested design examples
- Functional blocks can be saved in libraries as re-usable modules
- Robust design assistance features, such as merge, design estimation, place and route
- Utilities disassemble and convert common PAL*/GAL* JEDEC files into PDS source files.
- Functionally simulates designs using a powerful graphics waveform viewer
- Supports the SRAM architecture of FLEXlogic family of FPGAs
- Provides the best fit for Intel PLD and FPGAs



Product Description

PLDshell Plus is a powerful design entry and fitting tool for Intel's FLEXlogic family of FPGAs and iPLD line of devices. Hierarchical designs, merge and conversion capabilities, logic compilation, design simulation, a menuing interface—all a \$249 value, available FREE. These features and more make PLDshell the best no-risk method of evaluating Intel FPGAs and PLDs.

PLDshell Plus provides a cohesive package of design entry, logic compilation, design simulation and PAL/GAL JEDEC file conversion into PDS source files. It offers routing and fitting for Intel's entire line of iPLDs, consolidating multiple files and mapping them into one FPGA. PLDshell Plus accepts Boolean equation, state machine and truth table input formats, and simulation.

Hierarchical design entry is a feature of PLDshell Plus, improving design efficiency and allowing designs to be broken into functional blocks. Low-level modules can then be compiled and simulated before being integrated into a composite design. Libraries can be created so design modules can be reused.

The PLDshell Plus compiler offers the best fit for Intel PLD and FPGA architectures. Developed simultaneously with each new Intel device, the PLDshell Plus fitter is built specifically to optimize the powerful features of Intel's FPGAs and PLDs.

PLDshell Plus supports the greater design flexibility of the Intel FLEXlogic family of FPGAs and their SRAM-based architecture containing shadow PROM. For designs requiring the predictable speed, low-cost and ease-of-design of the iPLD line of small devices, PLDshell Plus offers its many powerful design features in the easiest-to-use design software on the market.

New PLDshell Plus users benefit from this no-risk, high-return evaluation opportunity. Run this easy-to-use design software and see the simplicity of designing with Intel's PLDs and FPGAs. Programming support for the FLEXlogic family of FPGAs is available by ordering the FLEXlogic Prototyping Cable Kit or the FLEXlogic Evaluation Kit through your local Intel sales representative or distributor.

System Requirements:

- Intel 386-based PC (or better) with 2 megabytes extended RAM
- MS-DOS 5.0 or later
- Hard disk space: 5 megabytes
- VGA monitor (for waveform viewing)
- Floppy disk drive: 1.44 megabytes

Features	Benefits
— Supports fitting to the iPLD line and the FLEXlogic family of FPGAs	— Both small and complex designs fit Intel devices with ease
— Merge, hierarchical design, conversion and menu interface plus conversion capabilities	— The easiest-to-use design software on the market — Efficient management of large designs
— Works with FLEXlogic Prototyping Cable Kit and FLEXlogic Evaluation Kit	— Designers can program Intel FPGAs without the investment of a programmer
— Capable of converting your PAL/GAL JEDEC files into PDS source files	— Conversion of existing design investments
— Functionally simulates designs	— Time saving verification of functionality of design
— Powerful graphics waveform viewer	— Faster analysis of simulation results

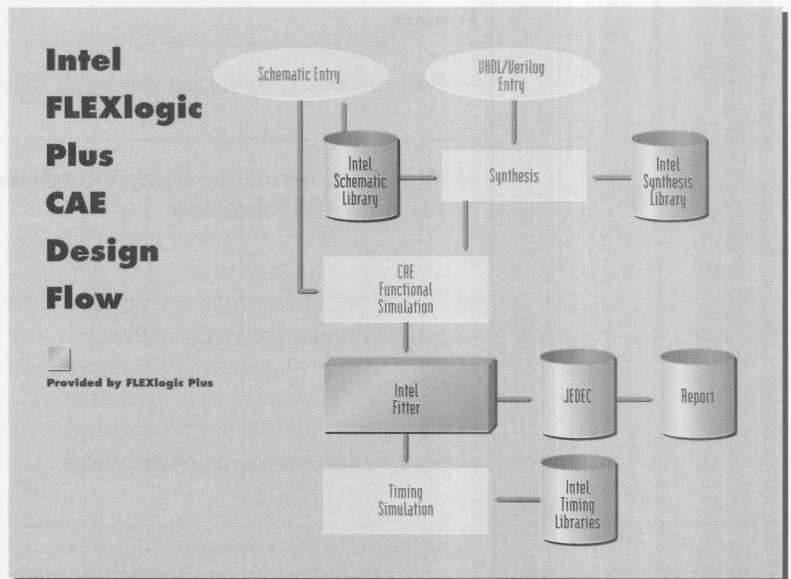
To request technical information, please return the reply card located within this booklet, or refer to the Information Resource card.

FLEXlogic Plus Design Kit

Product Brief

Product Highlights

- Supports Intel PLDs and FPGAs within Cadence, Mentor and Viewlogic
- Runs seamlessly within preferred vendor native environment
- Offers support for vendor VHDL and Verilog synthesis tools
- Device timing models provided for post-layout analysis
- Provides complete Intel design primitives library
- Supports leading platforms:
 - Sun Sparc
 - HP-700
 - Intel-based 486 PC; Pentium™ processor
- Technical support hotline available



Product Description

Intel's FLEXlogic Plus Design Kits are transparent to users working within the familiar framework of their preferred CAE environment. FLEXlogic Plus offers full-featured support for designs using Intel's FLEXlogic family of FPGAs or iPLD line. The Design Kits support quick, accurate design entry via schematic and HDL, and they offer complete compilation and timing simulation capabilities.

Intel's FLEXlogic Plus Design Kits offer comprehensive design support for Intel devices on Cadence, Mentor and Viewlogic systems. These powerful Design Kits provide design support starting with their own library of Intel design primitives and continuing on with synthesis support, functional simulation, compilation and timing simulation at the device and board or system levels.

The user interface of each Design Kit is customized to exactly match the vendor native environment. FLEXlogic Plus is the first completely clean, design environment offering such a tightly coupled design framework that time-consuming training time is eliminated.

A powerful feature of the FLEXlogic Plus Design Kit is its mixed-level design capability, allowing hierarchical schematics and textual design descriptions with a single design. Schematic entry is optimized by Intel's comprehensive Design Primitives Libraries. Textual design synthesis from VHDL or Verilog is supported through the Intel Synthesis Libraries provided.

FLEXlogic Plus uses Intel's own PLDasm router/fitter, ensuring the most efficient device utilization possible for your designs and providing the best fit for Intel architectures. Designs can be developed with FLEXlogic Plus, independent of a particular device architecture.

FLEXlogic Plus Design Kits enhance design productivity by offering two types of simulation support at the device or board levels: pre-fit functional simulation or post-fit timing simulation. The FLEXlogic Plus Design Kits provide highly accurate device timing models necessary for improving design productivity in post-layout analysis.

Features	Benefits
— Runs on Cadence, Mentor and Viewlogic CAE systems	— Designing with Intel devices supported on top three CAE vendor systems
— Menu-driven user interface is integrated right into your familiar CAE framework	— Has the same look and feel as the CAE environment you are accustomed to working with — Cohesive, seamless connectivity in designing with Intel's FLEXlogic Family of FPGAs or iPLD line.
— Supports Verilog and VHDL synthesis	— Flexibility in top-down, mixed-level design entry formats — All features of FLEXlogic FPGAs supported by Intel Synthesis Libraries
— Accurate device timing simulation models	— Supports accurate post-layout timing analysis — Supports timing simulation at the device and board or system levels
— Includes Intel's own PLDasm compiler	— Provides the best fit for your design within Intel architectures: 90% device utilization — Compiles most designs in under three minutes
— Comprehensive library of Intel Design Primitives provided	— Ensures easy-to-use, efficient, device utilization for schematic design entry
— On-line help and error messages	— Design Kits are easy to use — Short learning curve ensures high design productivity
— Robust reference and tutorial user guides provided	— Easy-to-find data for experienced users — Step-by-step design walk-through for new users

Hardware Requirements

Cadence:

Platform(s) supported: Sun Sparc

Hardware requirements: 5-10Mb disk space;

CAE memory requirements only

Software requirements: Version 4.2.1 and above

Distribution Media: QIC-24 Tape, tar format (Unix)

Mentor:

Platform(s) supported: Sun Sparc

Hardware requirements: 5-10Mb disk space;

CAE memory requirements only

Software requirements: Version 8.1 and above

Distribution Media: QIC-24 Tape, tar format (Unix)

Viewlogic:

Platform(s) supported: Sun Sparc, 486-PC

Hardware requirements: 5-10Mb disk space;

CAE memory requirements only

Software requirements: Version 4.1 and above

Distribution Media: QIC-24 Tape, tar format (Unix)

3 1/2" diskettes (DOS)

Hardware Requirements

Desktop:

Platform(s) supported: Sun Sparc
 Hardware requirements: 2-10MB disk space
 CAE memory requirements only
 Software requirements: Version 4.1.1 and above
 Distribution Media: QIC 34 Tape, or Remote (Linux)

Minitor:

Platform(s) supported: Sun Sparc
 Hardware requirements: 2-10MB disk space
 CAE memory requirements only
 Software requirements: Version 4.1 and above
 Distribution Media: QIC 34 Tape, or Remote (Linux)

VMEbus:

Platform(s) supported: Sun Sparc, 486-PC
 Hardware requirements: 2-10MB disk space
 CAE memory requirements only
 Software requirements: Version 4.1 and above
 Distribution Media: QIC 34 Tape, or Remote (Linux)
 VMEbus (DOS)

FPGA/PLD Fitter Kit

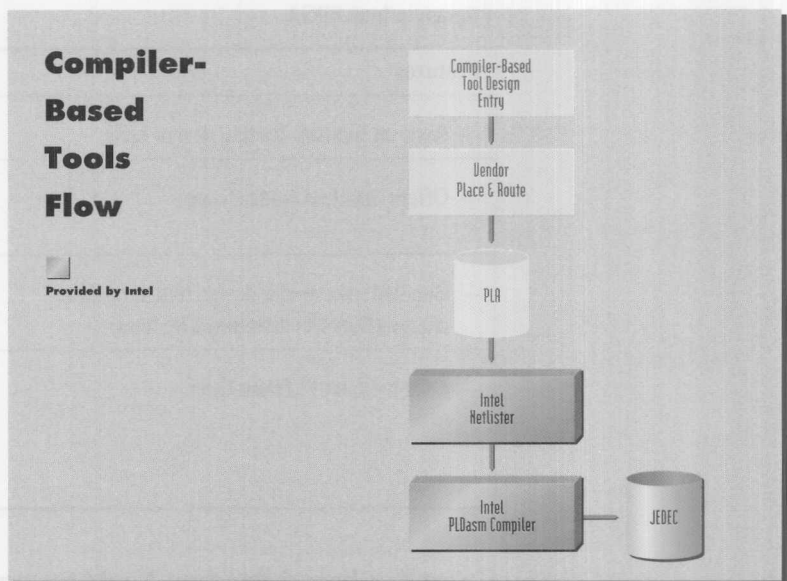
Product Brief

Product Highlights

- Use your preferred design tool to design with FLEXlogic FPGAs
- Transparent interface between Intel compiler and your existing design tool environment
- Supports leading FPGA/PLD design tool vendors: Data I/O, Logical Devices, Minc and OrCAD
- Uses the Intel PLDasm compiler, providing 90 percent device utilization in under three minutes
- Generates a working JEDEC file that is ready for programming
- Support for Intel devices bundled into compiler design tool at no extra charge to user

Compiler-Based Tools Flow

Provided by Intel



The Intel Fitter Kit Design Flow diagram illustrates the seamless connectivity between your preferred vendor design entry tool and the powerful PLDasm Intel compiler. The compiler-based tools supporting Intel's FLEXlogic family of FPGAs are teamed with Intel's advanced fitter technology to provide the fastest place and route for any FPGA.

Product Description

The Intel Fitter Kits support the FLEXlogic Family of FPGAs on the most popular design tools in the marketplace today: Data I/O, Logical Devices, Minc and OrCAD. The Fitter Kits offer a perfect mix of the vendor design tool technology and the powerful Intel PLDasm fitter — at no cost to the user.

To fully describe the integrated working partnership of the third-party tools and the Intel place and route tool, here is a step-by-step description of the Design Flow Diagram pictured above.

Compiler Tool Design Entry - The compiler-based design tool of your choice is used for design entry. All the dynamic features of Intel's FPGAs can be designed in using properties and keywords to take advantage of SRAM, COMPARATOR and other unique device capabilities.

Third-Party Place and Route - Designs targeted to Intel FPGAs are converted to PLA format by the vendor compiler. PLA format is an industry standard file format.

Intel Netlister - The Intel Netlister reads in the PLA representation of the design and converts it to PDS format suitable for the Intel PLDasm compiler.

Intel Compiler - The Intel PLDasm compiler does syntax checking, DT selection, minimizing, place and routing, and produces error and JEDEC files. (As a by-product of the fitting process, the Intel compiler produces the design in PDS format, which can be used by several of the CAE Design Kits offered by Intel.)

JEDEC - The Intel PLDasm compiler produces a JEDEC file that is ready to program in Intel FPGA.

Features	Benefits
— Runs on Industry leading design tools	— No costly learning curve to budget into design path
— Offers seamless connectivity	— Quick and easy to use — Saves design hassles of switching between software
— Bundled into vendor design tool at no extra charge (Data I/O distributed by Intel)	— Easy to order — No cost barrier to designing with Intel devices
— Uses the Intel PLDasm fitter	— 90% device utilization: the highest of any FPGA place and route tool — 3-minute compile time: the fastest place and route for an FPGA device

Compiler-based Product Features and Support Information

Logical Devices, Inc.

CUPL* — Total Designer

A high-level, universal design software package for PLDs and FPGA offerings:

- Variety of design expression formats
- True language flexibility
- DeMorgan expansion
- Simulation
- Output JEDEC Format
- Version 4.4 or above supports FLEXlogic

Deerfield Beach, FL (800) 331-7766

OrCAD*

OrCAD-PLD 386+

Software tool for programming PLDs and FPGAs. JEDEC Format output.

- Schematic entry from OrCAD SDT 386+
- Test vector generation
- 6 forms of input: Boolean equations, State Machines, Truth Tables, Streams, Indexed Equations, Numerical Maps
- Version 1.2 and above supports FLEXlogic FPGAs
- MS-DOS, Sun

Hillsboro, OR (503) 690-9881

Minc

PLDesigner-XL*

Discover how to solve your design challenge with Minc's unique optimization, design partitioning, and integration with your other EDA tools.

- Automated device selection based on user-specified design criteria
- Automatic partitioning across multiple PLDs
- Quick, easy retargeting between FPGA and PLD
- Functional simulation
- Import from high-level language, waveform editor, or schematic import
- Versions 3.1 and above support FLEXlogic

Colorado Springs, CO (800) 755-3742

DATA I/O

ABEL*

Designer software lets you describe and implement logic designs using behavioral language and can be simulated and converted into JEDEC standard format.

- Entry methods: ABEL*, Truth Table, State Machine, and Boolean Equation
- MS-DOS, Sun-3, Sun S, DEC VAX/VMS, Apollo*
- Intel FLEXlogic family supported under ABEL 4.3 and above through Intel PLD technical support, (800) 323-EPLD

Redmond, WA

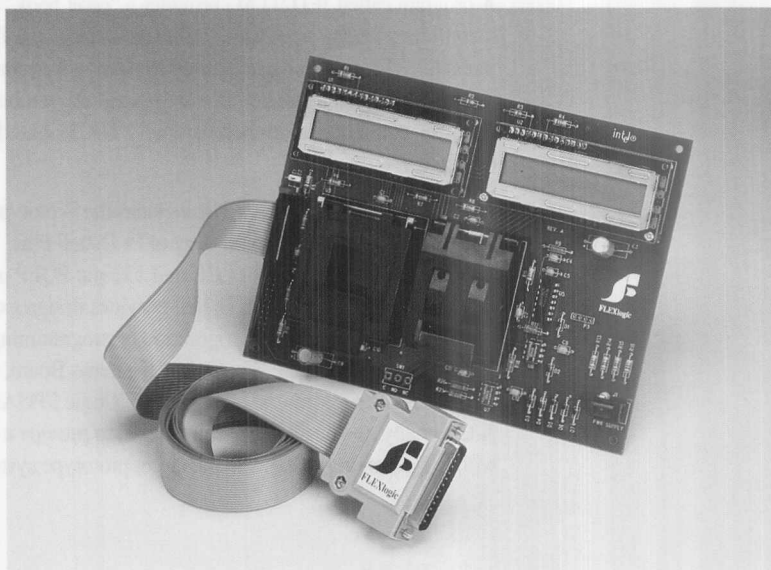
Call (800) 247-5700 for support.

Call the Intel Hotline for an ABEL Fitter Kit, (800) 628-2283.

FLEXlogic Prototyping Cable Kit and Evaluation Kit Product Brief

Product Highlights

- Program download into target prototype board via JTAG/IEEE 1149.1 standard interface cable and software
- Uses standard parallel printer port on any IBM-compatible PC
- Ability to program shadow EPROM on iFX780 devices
- Supports both 84-pin PLCC and 132-pin PQFP iFX780s
- Future growth path for in-circuit debug capability
- Includes software for custom loader circuits



Product Description

The architecture of Intel's FLEXlogic family of FPGAs provides you with flexible SRAM configurability and secure shadow EPROM non-volatile storage, both on one device. With in-circuit reconfiguration, the FLEXlogic designer can download new configuration files to the FPGA's SRAM-based volatile cells without removing the device from the application. This can be done as many times as desired, either for prototyping or as a requirement of the application.

In contrast, in-circuit programming allows the FLEXlogic designer to write a new configuration file to the built-in nonvolatile shadow EPROM cells of the FPGA so that the configuration will not be lost even when power is turned off. The configuration residing in the nonvolatile cells is automatically loaded into the FLEXlogic FPGA volatile cells upon power up.

Intel provides two levels of support for in-circuit reconfiguration and programming of the FLEXlogic family of FPGAs: the Prototyping Cable Kit and the Evaluation Kit.

The FLEXlogic Prototyping Cable Kit consists of the cable and software required to support in-circuit reconfiguration and programming of the Intel FLEXlogic family of FPGAs. The FLEXlogic devices support in-circuit reconfiguration and programming through the use of a standard JTAG/IEEE 1149.1 test port interface. The Prototyping Cable attaches to the parallel printer port of a PC and provides a 20-pin connector that interfaces to the board being prototyped. In addition to the standard JTAG interface signals, there are also pins provided for the future support of in-circuit debug capability.

The software provided with the FLEXlogic Prototyping Cable Kit supports multiple FLEXlogic FPGAs connected together in a chain along with other JTAG-compatible devices. The software can automatically detect, reconfigure and program FLEXlogic FPGAs within a chain while ignoring the other non-FPGA devices.

A program called JED2JTAG provides a "cook book" solution to iFX780 reconfiguration for users who don't want to learn the JTAG/IEEE 1149.1 interface in detail. This program can be used to painlessly reconfigure the iFX780 with JEDEC files from a number of storage sources: remote hard disk, on-board FLASH memory, communications port, or Intel's 80C51-based, low-cost downloader design example.

The FLEXlogic Evaluation Kit includes the Prototyping Cable hardware and software, a demo board, and a copy of PLDshell Plus. The demo board contains sockets for both the 84-pin PLCC and 132-pin PQFP packages used by the FLEXlogic iFX780 FPGA. The kit provides design examples and application notes that illustrate in-circuit reconfiguration or programming operations to the demo board. Since sockets are supplied on the demo Board, the Evaluation Kit can also be used as a device programmer for FLEXlogic FPGAs' on-chip shadow EPROM. Additionally, the demo board can be used to provide a JTAG communication link, with programming voltage, to the target prototype system.

To request technical information, please return the reply card located within this booklet, or refer to the Information Resource card.

FPGA/PLD Software Support

Vendor	Product	Features	Intel Kit	Devices Supported				
				FLEXlogic	iPLDxxx	85Cxxx	5Cxxx	5ACxxx
Cadence Design System 555 River Oaks Parkway San Jose, CA 95134 (408) 943-1234	Frameworks II 4.2.1	<ul style="list-style-type: none"> • Composer schematic capture • Verilog HDL using Synergy synthesis • Compilation • Timing simulation 	FLEXlogic Plus Design Kit for Cadence	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C22V10	5C032 5C060 5C090 5C180	5AC312 5AC324
	Abel 4.3	<ul style="list-style-type: none"> • Abel design language • Compilation • State-machine entry • Partitioning • Simulation 	PLDs supported in Abel; FLEXlogic supported by Intel FPGA/PLD Fitter Kit	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C22V10	5C032 5C060 5C090 5C180	5AC312 5AC324
Data I/O 10525 Willows Rd., NME PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700 (206) 881-6444 FAX (206) 882-1043	Abel 5.0	<ul style="list-style-type: none"> • Abel design language • Compilation • State-machine entry • Partitioning • Simulation • VHDL 	PLDs supported in Abel; FLEXlogic supported by Intel FPGA/PLD Fitter Kit	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C22V10	5C032 5C060 5C090 5C180	5AC312 5AC324
	PLDshell Plus	<ul style="list-style-type: none"> • FPGA/PLD Compiler • Functional simulator • Merge function • Timing 	N/A	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C22V10	5C032 5C060 5C090 5C180	5AC312 5AC324
ISDATA US/Canada: PO Box 19278 Oakland, CA 94619 (510) 531-8553 NON-US/Canada: Daimlerstr. 51 D-7500 Karlsruhe 21 Germany 721-751087	LOG/iC	<ul style="list-style-type: none"> • HINT VHDL synthesis • State View flow chart entry tool • Partitioner • Compiler 	No kit necessary; Support included in vendor base tool.			85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312

Vendor	Product	Features	Intel Kit	Devices Supported				
				FLEXlogic	iPLDxxx	85Cxxx	5Cxxx	5ACxxx
Logical Devices 692 S. Military Trail Deerfield Beach, FL 33442 1-800-331-7766	CUPL 4.4	<ul style="list-style-type: none"> • Compilation • Simulation 	No kit necessary; Support included in vendor base tool.	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C508	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
Logic Modeling 19500 NW Gibbs Dr. PO Box 310 Beaverton, OR 97075 1-800-344-0004	Smart Model	<ul style="list-style-type: none"> • Timing models for simulation 		iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090	5AC312 5AC324
Mentor 8005 SW Boeckman Rd. Wilsonville, OR 97070-777 (503) 685-7000	Falcon Framework 8.1	<ul style="list-style-type: none"> • Design Architect schematic capture • AutoLogic/VHDL Synthesis • Compilation • Quicksim II timing simulation 	FLEXlogic Plus Design Kit for Mentor	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
Minc, Inc. 6755 Earl Dr. Colorado Springs, CO 80918-1064 (719) 590-1155	PLDesigner v3.1	<ul style="list-style-type: none"> • Compilation • Simulation • VHDL • Partitioning 	No kit necessary; Support included in vendor base tool.	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C508	5C031 5C032 5C060 5C090 5C180	5AC312
OrCAD 3175 NW Alcock Dr. Hillsboro, OR 97124-7135 (503) 690-9881	OrCAD PLD386 + 2.0	<ul style="list-style-type: none"> • OrCAD/SDT 386 + schematic capture • Compilation • OrCAD/VST simulation 	No kit necessary; Support included in vendor base tool.	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
Viewlogic 293 Boston Post Road W. Marlboro, MA 01752 (800) 223-8429	Workview 4.1	<ul style="list-style-type: none"> • Viewdraw schematic capture • Compilation • Viewsim timing simulation 	FLEXlogic Plus Design Kit for Viewlogic	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224 85C508	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
	Workview Plus 5.1	<ul style="list-style-type: none"> • Viewdraw schematic capture • Compilation • Viewsim timing simulation 	FLEXlogic Plus Design Kit for Viewlogic	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
	Powerview 5.1	<ul style="list-style-type: none"> • Viewdraw schematic capture • Compilation • Viewsim timing simulation 	FLEXlogic Plus Design Kit for Viewlogic	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324

Vendor	Product	Features	Intel Kit	Devices Supported				
				FLEXlogic	iPLDxxx	85Cxxx	5Cxxx	5ACxxx
Viewlogic (Continued)	ViewPLD	<ul style="list-style-type: none"> • Workview schematic capture • Simulation • Abel compiler 	Intel FPGA/PLD Fitter Kit for compilation; FLEXlogic Plus Design Kit for Viewlogic for timing simulation	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
	Pro Series: Pro Sim	<ul style="list-style-type: none"> • Viewdraw schematic capture • Viewsim simulation • Waveform processing 	FLEXlogic Plus Design Kit for Viewlogic; must buy EDIF reader from vendor to support timing simulation	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324
	Pro Series: Pro Developer	<ul style="list-style-type: none"> • Viewdraw schematic capture • Abel compiler • Viewsim Simulation/waveform processing 	FLEXlogic Plus Design Kit for Viewlogic; must buy EDIF reader from vendor to support timing simulation	iFX780	iPLD610 iPLD910 iPLD22V10	85C220 85C224	5C031 5C032 5C060 5C090 5C180	5AC312 5AC324

FPGA/PLD Programming Support

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
Advin Systems Inc. 1050-L Duane Ave. Sunnyvale, CA 94086 (800) 627-2456 or (408) 243-7000 FAX (408) 736-2503	PILOT-U84	84-PIN Universal Programmer	PX-20 PX-28 PX-44 AM-1800 AM-78	iFX780 ⁽¹¹⁾ iFX740 ⁽¹¹⁾	DIP: iPLD610 iPLD910 iPLD22V10 PLCC: iPLD610 iPLD910 iPLD22V10	DIP: 85C060, 85C090 85C220, 85C224 85C22V10 PLCC: 85C060 ⁽²⁾ , 85C090 ⁽³⁾ 85C220 ⁽¹⁾ , 85C224 ⁽²⁾ 85C22V10 ⁽²⁾	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C180 ⁽⁴⁾ , 5C060 ⁽²⁾ 5C090 ⁽³⁾	DIP: 5AC312, 5AC324 PLCC: 5AC312 ⁽²⁾ 5AC324 ⁽³⁾
	PILOT-U40	40-PIN Universal Programmer	PX-20 PX-28 PX-44 AM-1800 AM-78	iFX780 ⁽¹¹⁾ iFX740 ⁽¹¹⁾	DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910	DIP: 85C060, 85C090 85C220, 85C224 85C22V10 PLCC: 85C060 ⁽²⁾ , 85C090 ⁽³⁾ 85C220 ⁽¹⁾ , 85C224 ⁽²⁾ 85C22V10 ⁽²⁾	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C180 ⁽⁴⁾ , 5C060 ⁽²⁾ 5C090 ⁽³⁾	DIP: 5AC312, 5AC324 PLCC: 5AC312 ⁽²⁾ 5AC324 ⁽³⁾
B & C Microsystems Inc. 750 N. Pastoria Ave. Sunnyvale, CA 94086 (408) 730-5511 FAX (408) 730-5521 BBS (408) 730-2317	PROTEUS-UP40	40 Pin Universal Programmer (DIP40)			DIP: PLD610 PLD910 PLCC: PLD610 PLD910	DIP: 85C060, 85C090 85C220 PLCC: 85C060, 85C090 85C220	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	PROTEUS-UPLC40	40 Pin Universal Programmer (DIP48 & PLCC84)			DIP: PLD610 PLD910 PLCC: PLD610 PLD910	DIP: 85C060, 85C090 85C220 PLCC: 85C060, 85C090 85C220	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	PROTEUS-UPLC56	56 Pin Universal Programmer (DIP48 & PLCC84)			DIP: PLD610 PLD910 PLCC: PLD610 PLD910	DIP: 85C060, 85C090 85C220 PLCC: 85C060, 85C090 85C220	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	PROTEUS-UPLC72	72 Pin Universal Programmer (DIP48 & PLCC84)			DIP: PLD610 PLD910 PLCC: PLD610 PLD910	DIP: 85C060, 85C090 85C220 PLCC: 85C060, 85C090 85C220	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	PROTEUS-UPLC88	88 Pin Universal Programmer (DIP48 & PLCC84)		iFX780	DIP: PLD610 PLD910 PLCC: PLD610 PLD910	DIP: 85C060, 85C090 85C220 PLCC: 85C060, 85C090 85C220	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324

FPGA/PLD Programming Support

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
Logical Devices, Inc. 692 S Military Trail Deerfield Beach, FL 33426 (800) 331-7766 (305) 428-6868 FAX (305) 974-8531	ALLPRO 88	Univ. 88-Pin + PLCC Socket Converter		iFX780	DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910	DIP: 85C220, 85C224 85C060, 85C090 PLCC: 85C220, 85C224 85C060, 85C090	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
Minato Electronics Inc. 3628 Madison Ave., #5 North Highlands, CA 95660 (916) 348-6066 FAX (916) 348-0926	1890A					DIP: 85C060, 85C090 85C220, 85C224 85C22V10 PLCC: 85C060, 85C090 85C220, 85C224 85C22V10	DIP: 5C031, 5C032 5C060, 5C090 5C121	DIP: 5AC312
Oliver Advanced Eng. 1146 N. Central Suite 380 Glendale, CA 91202 (818) 240-0080 FAX (818) 240-6131	OMNI-28	Univ. 28 Pins	OM-S-20 LCC OM-S-24 LCC		DIP: iPLD610 iPLD910 PLCC: iPLD610 ⁽⁷⁾ iPLD910	DIP: 85C220, 85C224 85C060, 85C090 PLCC: 85C220 ⁽⁶⁾ , 85C224 ⁽⁷⁾ 85C060, 85C090	DIP: 5C031, 5C032 5C060 PLCC: 5C060 ⁽⁷⁾	DIP: 5AC312
	OMNI-40	Univ. 40 Pin	OM-S-40 LCC		DIP: iPLD610 iPLD910 PLCC: iPLD610 ⁽⁷⁾ iPLD910 ⁽⁸⁾	DIP: 85C220, 85C224 85C060, 85C090 PLCC: 85C220 ⁽⁶⁾ , 85C224 ⁽⁷⁾ 85C060, 85C090	DIP: 5C031, 5C032 5C060, 5C090 5C121 PLCC: 5C090 ⁽⁸⁾ , 5C060 ⁽⁷⁾	
	OMNI-64	Univ. 68 Pins	OM-S-68 LCC		DIP: iPLD610 iPLD910 PLCC: iPLD610 ⁽⁷⁾ iPLD910 ⁽⁸⁾	DIP: 85C220, 85C224 85C060, 85C090 PLCC: 85C220 ⁽⁶⁾ , 85C224 ⁽⁷⁾ 85C060, 85C090	DIP: 5C031, 5C032 5C060, 5C090 5C121 PLCC: 5C090 ⁽⁸⁾ , 5C060 ⁽⁷⁾	

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
Data I/O 10525 Willows Road, N.E. P.O. Box 97046 Redmond, WA 98073 (800) 247-5700 (206) 881-6444 FAX (206) 882-1043	UNISITE 40/48	Univ. 20 to 68 Pins-CHIPSITE for PLCC	SITE 40/48		DIP: iPLD610 iPLD910	DIP: 85C220, 85C224 85C060, 85C090	DIP: 5C031, 5C032 5C060, 5C090	DIP: 5AC312, 5AC324 ⁽⁵⁾
			CHIPSITE		PLCC: iPLD610 iPLD910	PLCC: 85C220, 85C224 85C060, 85C090	PLCC: 5C060, 5C090 5C180	PLCC: 5AC312 5AC324
			PPI Base	IFX780				
			PPI Base with Adaptor #0527	IFX780				
	Model 2900	Univ. 44 Pin			DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910	DIP: 85C220, 85C224 85C060, 85C090 PLCC: 85C220, 85C224 85C060, 85C090	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090 5C180	DIP: 5AC312, 5AC324 ⁽⁵⁾ PLCC: 5AC312 5AC324
			PPI Base with Adaptor #0527	IFX780				
			PPI Base with Adaptor #0229	IFX780				
	Model 3900	Univ. 84 Pins			DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910	DIP: 85C220, 85C224 85C060, 85C090 PLCC: 85C228, 85C224 85C060, 85C090	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
Elan Systems 365 Woodview Ave. Suite 700 Morganhill, CA 95037 (800) 541-3526 (408) 778-7267 FAX (408) 778-2597 Elan Digital Systems Ltd. Elan House, Little Park Farm Road, Segensworth West, Fareham, Hampshire P0155SJ Q489 579799 Q489 577516	5-145	Programmer + PLCC Socket Converters			DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910		DIP: 5C032, 5C060 5C090, 5C031 PLCC: 5C060, 5C031 5C090, 5C032 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	6000	Univ. Pin Driven Programmer			DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910	DIP: 85C220, 85C224 85C22V10 85C060, 85C090 PLCC: 85C220, 85C224 85C22V10 85C060, 85C090	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C031, 5C032 5C060, 5C090	DIP: 5AC312 PLCC: 5AC312

FPGA/PLD Programming Support

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
BP Microsystems 1000 N Post Oak Road Houston, TX 77055-7237 (800) 225-2102 or (713) 688-4600 FAX (713) 688-0920 BBS (713) 688-9283	PLD-1128	28 Pins + PLCC Socket Converter (Only supports PLDs)			DIP: iPLD610 iPLD910 iPLD22V10 PLCC: iPLD610 iPLD910 iPLD22V10	DIP: 85C060, 85C090 85C220, 85C224 85C960 85C22V10 PLCC: 85C060, 85C090 85C220, 85C224 85C22V10 85C960	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	CP-1128	28 Pins + PLCC Socket Converter (Supports PLDs, EPROMs, and EEPROMs)			DIP: iPLD610 iPLD910 iPLD22V10 PLCC: iPLD610 iPLD910 iPLD22V10	DIP: 85C060, 85C090 85C220, 85C224 85C960 85C22V10 PLCC: 85C060, 85C090 85C220, 85C224 85C960 85C22V10	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	BP-1200	Supports up to 240 Pins (both PQFP and PLCC)		IFX780	DIP: iPLD610 iPLD910 iPLD22V10 PLCC: iPLD610 iPLD910 iPLD22V10	DIP: 85C060, 85C090 85C220, 85C224 85C960 85C22V10 PLCC: 85C060, 85C090 85C220, 85C224 85C960 85C22V10	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C060, 5C090 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	PLD-1100	20/24 Pins + PLCC Socket Converters			DIP: PLD610 PLD22V10 PLCC: PLD610 PLD22V10	DIP: 85C060, 85C090 85C220 84C22V10 PLCC: 85C060, 85C090 85C220 85C22V10	DIP: 5C031, 5C032 5C060 PLCC: 5C060	DIP: 5AC312 5AC324 PLCC: 5AC312
Bytek Corp. Instrument Systems Div. 543 N.W. 77th Street Boca Raton, FL 33487 (800) 523-1565 (407) 994-3520 FAX (407) 994-3615	135H-U	Universal MULTIPROGRAMMER	UNICEL w/LTA00C		DIP: iPLD610 iPLD910	DIP: 85C220, 85C224 85C060, 85C090	DIP: 5C031, 5C032 5C060, 5C090	DIP: 5AC312
	145H-U	Logic Programmer			DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910	DIP: 85C220 85C224 85C060 85C090	DIP: 5C031, 5C032 5C060, 5C090	DIP: 5AC312

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
SMS North America, Inc. P.O. Box 3159 Redmond, WA 98073-8447 (206) 883-8447 FAX (206) 883-8601 BBS (206) 867-5437	Sprint Expert	Univ. 48 Pin Driver Univ. programming support for microcontrollers, logic memory, and related devices	DIP: Top 40 or 48 PLCC: Top 3, Top 44 or Top 1		DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910	DIP: 85C060, 85C090 85C220, 85C224 85C508 85C22V10 PLCC: 85C060, 85C090 85C220, 85C224 85C508 85C22V10	DIP: 5C031, 5C032 5C060, 5C090 5C121, 5C180 PLCC: 5C031, 5C032 5C060, 5C090 5C121, 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	Sprint Optima	Univ. 48 Pin Driver Univ. programming support for microcontrollers, logic memory, and related devices	DIP: Top 40 or 48 PLCC: Top 3, Top 44 or Top 1		DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910	DIP: 85C060, 85C090 85C220, 85C224 85C508 85C22V10 PLCC: 85C060, 85C090 85C220, 85C224 85C508 85C22V10	DIP: 5C031, 5C032 5C060, 5C090 5C121, 5C180 PLCC: 5C031, 5C032 5C060, 5C090 5C121, 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	Multisite	Univ. 48 Pin Driver Univ. GANG	DIP: Top 40 or 48 PLCC: Top 3, Top 44 or Top 1		DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910	DIP: 85C060, 85C090 85C220, 85C224 85C508 85C22V10 PLCC: 85C060, 85C090 85C220, 85C224 85C508 85C22V10	DIP: 5C031, 5C032 5C060, 5C090 5C121, 5C180 PLCC: 5C031, 5C032 5C060, 5C090 5C121, 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	Sprint Plus 48	Univ. 48 Pin Driver (Low Cost)	48 Pin Socket PLCC Adapters		DIP: iPLD610 iPLD910 PLCC: iPLD610 iPLD910	DIP: 85C060, 85C090 85C220, 85C224 85C508 85C22V10 PLCC: 85C060, 85C090 85C220, 85C224 85C508 85C22V10	DIP: 5C031, 5C032 5C060, 5C090 5C121, 5C180 PLCC: 5C031, 5C032 5C060, 5C090 5C121, 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324

Vendor	Product	Product Description	Module	Devices Supported				
				FLEXlogic	iPLD	85Cxxx	5Cxxx	5ACxxx
Stag Microsystems, Inc. 1600 Wyatt Drive, Suite 3 Santa Clara, CA 95054 (408) 988-1118 FAX (408) 988-1232	ZL-30A	Logic 28 Pin + PLCC Adaptor	30A640				DIP: 5C031, 5C032 5C060, 5C090 ⁽¹⁰⁾ PLCC⁽¹⁰⁾: 5C060, 5C090	DIP: 5AC312 PLCC⁽¹⁰⁾: 5AC312
	System 3000				DIP: iPLD610 iPLD910	DIP: 85C220, 85C224 85C060, 85C090	DIP: 5C031, 5C032 5C060, 5C090	DIP: 5AC312
	ZL30B	Univ. 28 Pin + PLCC (Larger Library)			DIP: iPLD610 iPLD910	DIP: 85C220, 85C224 85C22V10 85C060, 85C090	DIP: 5C031, 5C032 5C060, 5C090	DIP: 5AC312
System General Corp. 510 S. Park Victoria Drive Milpitas, CA 95035 (408) 263-6667 FAX (408) 262-9227	TURPRO-1	Univ. 84-Pin Programmer	PLCC Adaptor: P28 P32 P44 P68 P84		DIP: iPLD610 iPLD910	DIP: 85C220, 85C224 85C060, 85C090 PLCC: 85C060, 85C090 85C220, 85C224 85C22V10	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C031, 5C032 5C060, 5C090 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
	TURPRO/FX	Univ. 84 Pin Programmer	PLCC Adaptor: P28 P32 P44 P68 P84		DIP: iPLD610 iPLD910	DIP: 85C220, 85C224 85C22V10 85C060, 85C090 PLCC: 85C060, 85C090 85C220, 85C224 85C22V10	DIP: 5C031, 5C032 5C060, 5C090 PLCC: 5C031, 5C032 5C060, 5C090 5C180	DIP: 5AC312 5AC324 PLCC: 5AC312 5AC324
Xeltek 757 North Pastoria Ave. Sunnyvale, CA 94086 (408) 524-1929 FAX (408) 245-7084	SUPERPRO	40-Pin Univ. Programmer				DIP: 85C060, 85C090 85C220, 85C224 85C22V10 PLCC: 85C060, 85C090 85C220, 85C224 85C22V10	DIP: 5C031, 5C032 5C060, 5C090 5C180 PLCC: 5C031, 5C032 5C060, 5C090 5C180	DIP: 5AC312 PLCC: 5AC312

NOTES:

1. With PX-20
2. With PX-28
3. With PX-44
4. With AM-1800
5. SITE 48 only
6. With OM-S-20 LCC
7. With OM-S-24 LCC
8. With OM-S-40 LCC
9. With OM-S-68 LCC
10. With 30A640
11. With AM-78

FPGA and PLD Support At-a-Glance

Intel			Data IO*				Logical Devices	
PLD	Packages	PLDshell Plus S/W	ABEL* S/W	UNISITE*	Model 2900	Model 29B LogicPak*	CUPL S/W	ALLPRO 40/88
85C220-100/80/66	D, P N, M	V3.1	V3.2	SITE40/48 (V2.8) CHIPSITE (V3.0)	V1.1 V1.1	303A-011A (V10) 303A-011B (V05)	V3.2	1.50c 1.50c
85C220-7/10	N	V3.1	V3.2	CHIPSITE (V3.0)	V1.1	303A-011B (V05)	V3.2	1.50c
85C224-100/80/66	D, P N, M	V3.1	V4.0	SITE40/48 (V3.1) CHIPSITE (V3.1)	V1.2 V1.2	303A-011A (V14) 303A-011B (V06)	V4.0	2.1 2.1
85C224-7/10	N	V3.1	V4.0	CHIPSITE (V3.1)	V1.2	303A-011B (V06)	V4.0	2.1
85C22V10	D, P N	V3.1	V4.2	SITE40/48 (V3.7) CHIPSITE (V3.7)	V1.8 V1.8	303A-011A (V18) 303A-011B (V06)	V4.0	— —
5AC312	D, P N, M	V3.1	V4.0	SITE40/48 (V2.2) PINSITE (V3.0)	V1.0 V1.1	303A-011A (V07) 303A-011B (V06)	V3.2	V1.48 V1.48
5AC324	D, P N	V3.1	V3.2	SITE40/48 (V3.2) PINSITE (V3.3)	V1.5 V1.5	n/s n/s	V3.2	V1.50 V1.50
5C031	D	V3.1	V3.0	SITE40/48 (V1.7)	V1.0	303A-011A (V02)	V2.15	V1.46
5C032	D, P	V3.1	V3.0	SITE40/48 (V1.2)	V1.0	303A-011A (V02)	V2.15	V1.46
5C060	D, P N, M	V3.1	V3.0	SITE40/48 (V2.7) CHIPSITE (V2.7)	V1.0 V1.1	303A-011A (V01) 303A-011B (V01)	V2.15	V1.46 V1.46
5C090	D, P N, M	V3.1	V3.0	SITE40/48 (V2.7) CHIPSITE (V2.7)	V1.0 V1.1	303A-010 (V03) 303A-010 (V03)	V2.50	V1.46 V1.46
5C180	N, M	V3.1	V3.0	CHIPSITE (V2.7)	n/s	n/s	V3.0	V1.46

FPGA and PLD Support At-a-Glance

Intel			Data IO*				Logical Devices	
PLD	Packages	PLDshell Plus S/W	ABEL* S/W	UNISITE*	Model 2900	Model 29B LogicPak*	CUPL S/W	ALLPRO 40/88
FX780	KU N	V3.1	unknown	PINSITE (V4.3)	V3.1 V3.2	n/s	unknown	unknown
PLDLV22V10	P N	V3.1	unknown	SITE40/48 (V4.3) PINSITE (V4.3)	V3.2 V3.2	n/s	unknown	unknown
PLD22V10	P N	V3.1	V4.0 ⁽¹⁾	SITE40/48 (V3.8) CHIPSITE (V3.8)	V1.9 V1.9	303A-010 (V18) 303A-010 (V08)	V4.0 ⁽¹⁾	2.2 2.2
PLD610	P N	V3.1	V3.0 ⁽²⁾	SITE40/48 (V3.8) CHIPSITE (V3.8)	V1.9 V1.9	303A-011A (V14) 303A-011B (V06) ⁽²⁾	V2.15 ⁽²⁾	2.2 2.2
PLD910	P N	V3.1 ⁽³⁾	V3.0 ⁽³⁾	SITE40/48 (V3.8) CHIPSITE (V3.8)	V1.9 V1.9	303A-010 (V03) 303A-010 (V03) ⁽³⁾	V2.50 ⁽³⁾	2.2 2.2



Model 3900: All devices supported with V1.2 (NOW)

NOTES:

1. Complete support provided as 85C22V10
 2. Complete support provided as 85C060
 3. Complete support provided as 85C090
- n/s = Will not be supported due to hardware limitation.

*Data I/O = 1-800-3-DATAIO

Logical Devices = 1-800-331-7766

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CUPL and ALLPRO are trademarks of Logical Devices, Inc.

Ordering Information

To place an order contact your local distributor and refer to the following product order codes:

PLD	Order Code	Package
iFX780	KUFX780-10	132 pin PQFP
	NFX780-10	84 pin PLCC
	KUFX780-15	132 pin PQFP
	NFX780-15	84 pin PLCC
iFX780Z	KUFX780Z-10	132 pin PQFP
	NFX780Z-10	84 pin PLCC
	KUFX780Z-15	132 pin PQFP
	NFX780Z-15	84 pin PLCC

iFX740	N68FX740-10	68 pin PLCC
	N44FX740-10	44 pin PLCC
	N68FX740-15	68 pin PLCC
	N44FX740-15	44 pin PLCC
iFX740Z	N68FX740Z-10	68 pin PLCC
	N44FX740Z-10	44 pin PLCC
	N68FX740Z-15	68 pin PLCC
	N44FX740Z-15	44 pin PLCC

iPLD22V10	P PLD22V10-7	PDIP
	N PLD22V10-7	PLCC
	P PLD22V10-10	PDIP
	N PLD22V10-10	PLCC
	P PLD22V10-15	PDIP
	N PLD22V10-15	PLCC
	P PLD22V10-25	PDIP
	N PLD22V10-25	PLCC

iPLDLV22V10	P PLDLV22V10-15	PDIP
	N PLD22V10-15	PLCC

Support Tool	Order Code
FLEXlogic Prototyping Cable Kit	EVFX780CBL

Support Tool	Order Code	Delivery
FLEXlogic Evaluation Kit	EVFX780US	United States
	EVFX780E	European
	EVFX780J	Japan

Support Tool	Order Code	Support For
FLEXlogic Design Kit	FXDKCDNCE	Cadence
	FXDKMNTR	Mentor
	FXDKVLGC	Viewlogic

iPLD610	D PLD610-10	PDIP
	N PLD610-10	PLCC
	P PLD610-10	PDIP
	TN PLD610-12	PLCC
	D PLD610-15	PDIP
	N PLD610-15	PLCC
	P PLD610-15	PDIP
	TD PLD610-15	†CerDIP
	TN PLD610-15	PLCC
	D PLD610-25	PDIP
	N PLD610-25	PLCC
	P PLD610-25	PDIP
	TD PLD610-25	†CerDIP
	TN PLD610-25	PLCC

iPLD910	D PLD910-12	PDIP
	N PLD910-12	PLCC
	P PLD910-12	PDIP
	TN PLD910-12	PLCC
	D PLD910-15	PDIP
	N PLD910-15	PLCC
	PLD910-15	†CerDIP
	TN PLD910-15	PLCC
	D PLD910-25	PDIP
	N PLD910-25	PLCC
	P PLD910-25	PDIP
	TP PLD910-25	†CerDIP
	TN PLD910-25	PLCC

85C220	N85C220-100	PLCC
	D85C220-80	†CerDIP
	P85C220-80	PDIP
	N85C220-80	PLCC
	D85C220-66	†CerDIP
	P85C220-66	PDIP
	N85C220-66	PLCC
	N85C220-7	PLCC
	P85C220-7	PDIP
	N85C220-10	PLCC
	P85C220-10	PDIP

85C224	N85C224-100	PLCC
	D85C224-80	†CerDIP
	P85C224-80	PDIP
	N85C224-80	PLCC
	D85C224-66	†CerDIP
	P85C224-66	PDIP
	N85C224-66	PLCC
	N85C224-7	PLCC
	P85C224-7	PDIP
	N85C224-10	PLCC
	P85C224-10	PDIP

5AC312	D5AC312-25	†CerDIP
	P5AC312-25	PDIP
	N5AC312-25	PLCC
	D5AC312-30	†CerDIP
	P5AC312-30	PDIP
	N5AC312-30	PLCC

5AC324	N5AC324-25	PLCC
	P5AC324-25	PDIP
	D5AC324-25	†CerDIP
	N5AC324-30	PLCC
	P5AC324-30	PDIP
	D5AC324-30	†CerDIP

†Windows package allows UV erase

